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WAVETEK

WAVETEK SAN DIEGO, INC.

9045 Balboa Ave., San Diego, CA 92123

INSTRUCTION MANUAL

MODEL 112

TRIGGERED VCG

MODEL 115

PHASE LOCK/TRIGGER VCG

MODEL 116

MULTI-PURPOSE VCG

This manual provides descriptive material and instructions for the installation, operation, maintenance, and repair of this instrument. Wavetek's product improvement program ensures that the latest electronic developments are incorporated in all Wavetek instruments by the addition of circuit and component changes as rapidly as development and testing permit. Due to the time required to document and print instruction manuals, it is not always possible to incorporate the more recent changes in the released manual. In this case, data will be found on engineering change sheets at the front of the manual. If no change sheets are included, the manual is correct as printed.

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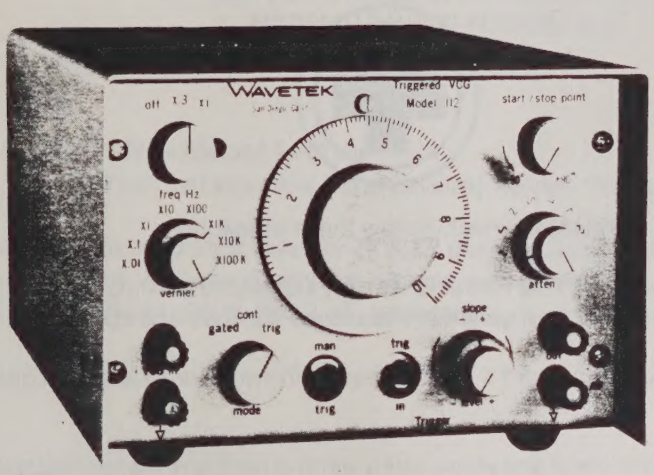
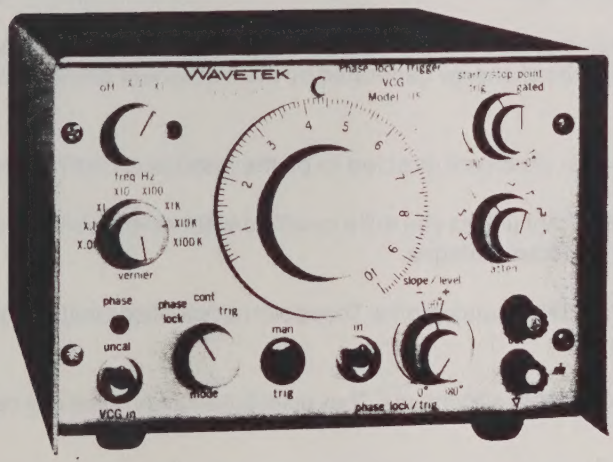




Models 112, 115, 116
Function Generators

SAFETY FIRST

Protect yourself. Follow these precautions:

- Don't touch the outputs of the instrument or any exposed test wiring carrying the output signals. This instrument can generate hazardous voltages and currents.
- Don't bypass the power cord's ground lead with two-wire extension cords or plug adaptors.
- Don't disconnect the green and yellow safety-earth-ground wire that connects the ground lug of the power receptacle to the chassis ground terminal (marked with ⏚ or ⚠).
- Don't hold your eyes extremely close to an rf output for a long time. The normally nonhazardous low-power rf energy generated by the instrument could possibly cause eye injury.
- Don't plug in the power cord until directed to by the installation instructions.
- Don't repair the instrument unless you are a qualified electronics technician and know how to work with hazardous voltages.
- Pay attention to the **WARNING** statements. They point out situations that can cause injury or death.
- Pay attention to the CAUTION statements. They point out situations that can cause equipment damage.

INSTRUCTION MANUAL ADDENDUM
–For–
MODEL 112 TRIGGERED VCG
MODEL 115 PHASE LOCK/TRIGGER VCG
MODEL 116 MULTI-PURPOSE VCG

Page 2-6 Square Wave Rise and Fall Time

Delete 5 volt adjustable (battery models) less than 100 nsec.

Acceptable substitute for Elpac capacitor ZX3022. Due to procurement problems, the Elpac ZX3022 capacitor (five per instrument) may be replaced with American Radionics capacitor 5WVTK-2MFW2106F (matched set of five 2 μF capacitors).

SECTION I
GENERAL DESCRIPTION AND OPERATION

GENERAL

The WAVETEK Model 112 Triggered VCG and the Model 115 Trigger/Phase Lock VCG are semi-precision sources of waveforms from servo to video frequencies. These units are extremely rugged, completely transistorized portable packages. They feature complete plug-in printed circuit board construction with interchangeable individually calibrated PC boards utilizing silicon semiconductors throughout. The extremely clean and stable waveform signals from 0.0015 Hz to 1 MHz makes these generators highly versatile general purpose pieces of equipment for the laboratory or the field.

The Models 112 and 115 are identical in size and performance except that the Model 115 offers phase lock capabilities in addition to the trigger capabilities of the Model 112. Both models feature a main output with function selector switch and amplitude attenuator, and in addition, simultaneous 5 volt peak to peak 50Ω outputs of sine, square and triangle waveforms and 2.5 volt peak ramp waveform. In addition they offer a 1 volt 10 nsec. rise and fall time square wave and -10 volt sync pulse. There is also a selectable differential output that provides signals identical to but 180° out of phase with the fixed sine, square, triangle and ramp output waveforms. The main output can be selected to be in phase or 180° out of phase with the fixed outputs. Frequency is controlled by an eight position range switch at 20:1 range thus providing good overlap.

All outputs may be shorted simultaneously and the generator will continue to oscillate internally with less than 0.5% change in frequency. Voltage may be applied back into the generator so long as this voltage does not exceed the maximum output voltage. Up to ± 50 volts may be applied to the VCG input without damage.

MODEL 112

The Model 112 features VCG voltage control of frequency by the internal frequency dial operating in parallel with the VCG input terminals. The generated frequency is the resultant sum of the VCG input voltage and the dial setting. Without an externally applied voltage, the dial governs and the generator operates like the basic WAVETEK function generator, the Model 110. By adding a positive voltage to the input terminals, the frequency is increased; by adding a negative voltage to the input terminals, the frequency is decreased. The applied voltage may be either a DC programming voltage or an AC frequency modulating voltage. The modulation band width is 100 KHz (it is possible to have a higher modulation frequency than carrier frequency, with a resultant triangle wave that may look like a staircase).

The frequency dial is a continuously variable quality composition potentiometer. An electronic frequency vernier is incorporated for extremely precise frequency adjustment. The vernier covers one minor dial division for one vernier rotation.

In addition to sine, square and triangle, the Model 112 also offers ramp functions. The base line of this ramp signal is 0 volts and the ramp duty cycle is 50%. The ramp available on the front panel binding post can be selected to be positive or negative going. The ramp on the fixed BNC connector on the rear panel is a negative ramp and the ramp available on the differential output on the rear panel when selected is a positive going ramp.

MODELS 112 and 115; MODELS 112B and 115B

The Models 112 and 115 incorporate a power amplifier which offers the maximum of 32.5 volts peak to peak (plus or minus 16.25 volt ramp) at the front panel binding post output. An attenuator is included on the input of this output amplifier. The amplifier will supply 30 volts peak to peak (15 volt ramp) into a 600Ω load at maximum output setting. Ten volts peak to peak (5 volt ramp) may be driven into a 50Ω load with undistorted waveform by rotating the output attenuator counter-clockwise until clipping no longer occurs. Very low impedance loads can be driven without distortion by further rotation of the output attenuator in the counter-clockwise direction.

NOTE

When a relatively low output signal is needed, it is recommended that the output be attenuated by an external pair of resistors to a level approximating that required and the internal attenuator be used as the amplitude vernier. Attenuating the output by 10:1, 100:1, or 1000:1, etc. The use of a pair of external resistors will insure clean waveform quality and good resolution by the internal attenuator in low level applications.

The Models 112B and 115B incorporate an internal battery charger in place of the power amplifier. These units will operate continuously for eight hours from the internal batteries. Both may be charged completely in 16 hours. The charger is designed so that charging occurs while the unit is in operation. A screwdriver adjustment enables the operator to set the desired charge rate. In the maximum clockwise position, the charge time from discharge to charge is 14 hours. Frequent operation with the instrument plugged into AC power with the charge rate set this high could result in damage to the batteries. The maximum counter-clockwise position of the rear control sets the charge rate to maintain the batteries at full charge without overcharge. The units are wired so that when plugged into AC power, but turned off, a trickle charge maintains the batteries at full charge setting.

The power amplifier used in the Model 112 and 115 is not utilized in the 112B and the 115B and is thus bypassed. The signal appearing on the binding post in the 112B and 115B is a maximum 5 volt peak to peak (2.5 volt ramp) at a 600Ω ±20% output impedance.

MODELS 112 and 112B; CONTROLS AND TERMINALS

Controls and outputs for the Models 112 and 112B are identical except for the output impedances and voltage levels at the binding posts. For the Model 112, these are 50Ω and 0.600 to 30 volts peak to peak (or, by removing one jumper, an impedance of 600Ω is obtained. Output impedance of the Model 112B is 600Ω ±20% at voltage levels of 0.100 to 5 volts peak to peak (zero to 2.5 volts peak to peak ramp). No zero adjustment is provided for this output on the Model 112B, but internal controls permit setting of the balance of each function independently.

POWER/DIAL MULTIPLIER SWITCH

This switch incorporates two ON positions, X.3 and X1. This switch in conjunction with the frequency range switch and the frequency dial, determines the generated frequency. For example, if the dial is set at 3.5, the frequency range switch setting at X100, and the dial multiplier switch at X1, the generated frequency is 350 Hz. With the dial multiplier switch at X.3, the frequency is 105 Hz.

In the Model 112B, when the switch is in the OFF position, the batteries are disconnected from the instrument but connected to the charger. In this position, the charger is set for a trickle charge when the instrument is connected to line power. In the ON position, the batteries are connected to the instrument for normal operation. If the instrument is not connected to the line power, the batteries are discharging; but, if connected, the charger supplies sufficient current to operate the instrument and charge the batteries. The amount of charge current available is variable through the potentiometer at the rear panel. In the maximum counter-clockwise rotation, the charge current is minimum. In the maximum clockwise position, the charge current is maximum. The maximum counter-clockwise position is recommended for optimum battery life unless maximum charge rate is required due to duty use cycle.

CAUTION

If the batteries are allowed to completely discharge, the instrument power supply cannot provide adequate power to simultaneously operate and charge. If this condition exists, the instrument should be allowed to recharge for a period of time before it is used in the AC mode.

FREQUENCY RANGE SWITCH

The frequency range switch selects the appropriate timing resistor and capacitor for proper frequency range.

FREQUENCY DIAL AND FREQUENCY VERNIER

The frequency dial is a high quality composition potentiometer providing continuous frequency control. In addition, an electronic vernier control is provided for precise frequency setting. Complete rotation of the vernier changes the frequency approximately one minor dial division for all settings of the dial. The frequency vernier should be in the extreme clockwise position ("cal") for maximum dial accuracy.

FUNCTION SELECTOR SWITCH, OUTPUT ATTENUATOR, and DC ZERO ADJUST (rear-mounted screwdriver adjustment).

The main output impedance is 50Ω, but the output current is limited to drive approximately ±100 ma into a short circuit. The output at maximum clockwise attentuator position is 32.5 volts peak to peak open circuit and 30 volts peak to peak into a 600Ω load. If the load impedance is less than 600Ω, the attenuator must be rotated counter-clockwise or clipping will result. Maximum undistorted output into a 50Ω load is 10 volts peak to peak.

The output attenuator covers a 30 db range. For output voltages less than 20 db below maximum output, it is recommended that an external attenuator using a pair of resistors be used and the internal attenuator be used as a fine control. For a 10:1 attenuator, use a 470Ω resistor in series with a 56Ω resistor in shunt with the load. For a 100:1 attenuator, use a 1K resistor in series and a 10Ω resistor in shunt with the load; or, 4.7KΩ in series and a 51Ω resistor in shunt with the load (these values are indicative and not critical). The attenuator is located in the input of the output amplifier. As a result, the zero adjust will be most critical at minimum setting. The rear-mounted dc adjustment control should be adjusted with the attenuator in the maximum counter-clockwise position.

The function selector switch selects the function delivered to the main power amplifier and also selects the output available on the differential output BNC connector on the rear panel. The signal delivered to the selected differential output connector on the rear panel is always 180° out of phase with the associated fixed output on the rear panel no matter what position the function selector switch is in. The output delivered to the front panel binding post, however, can be selected to be in phase or 180° out of phase with the signal delivered to the fixed output BNC connectors on the rear panel.

NOTE

Zero adjust control is a high resolution Zero Adjust Potentiometer, not a dc offset control. A minor modification, however, will allow this control to be used as a dc offset control (see detailed circuit description).

Switch selected sine, square, and triangle waves will have equal peak to peak amplitude for all attenuator settings.

THE 5V TRIANGLE, 5V SINE and 5V SQUARE OUTPUTS

These outputs are accurate 5 volt, 50Ω sources balanced about ground. They will drive 2.5 volts peak to peak into a 50Ω load and supply ±50 ma peak into a short circuit.

THE 10 NSEC. SQUARE WAVE OUTPUT

The 10 nsec. square wave output is approximately 1 volt peak to peak open circuit, and 0.5 volts peak to peak into a 50Ω load with better than 10 nsec. rise and fall time. Always use a 50Ω cable and a 50Ω termination when using this output.

SYNC OUTPUT

At least -10 volts sync signal, less than 5 μsec. in pulse width (typically 1.5 μsec. pulse width). The pulse occurs once per cycle coincident with the positive transition of the 5 volt square wave and the positive peak of the sine and triangle waves.

NOTE

Due to its very narrow pulse width, the sync pulse is difficult to observe at low frequencies. However, it will trigger wide band oscilloscopes such as the Tektronix Model 453 at all frequencies.

MINUS 2.5 VOLT PEAK RAMP

The ramp output is a minus going 2.5 volt output whose base line is at zero volts ±25 mv (5 mv, typical). Open circuit voltage is a 2.5 volt negative going ramp with a duty cycle of 50%. The negative ramp coincides in time with the negative going portion of the triangle wave and the positive half of the square wave.

VCG INPUT

The VCG input permits remote control of dial frequency and frequency modulation. The calibration factor is 0.5 volts per major dial division. A positive voltage causes an increase in frequency and a negative voltage causes a decrease. The setting of the frequency dial (and the frequency vernier) determines the base frequency. The VCG input impedance is 10KΩ. Up to ±50 volts can be applied to the VCG input without damage.

GATED/CONTINUOUS/TRIGGER MODE SWITCH

The mode switch selects the desired mode of operation. In the continuous mode the generator runs continuously and cannot be gated or triggered. In the triggered mode the generator does not give an output until the manual trigger button is depressed or

an appropriate triggering signal is applied to the front panel. When a triggering signal is received or the manual trigger is depressed, one cycle will be generated on command, the starting point of which will be determined by the start-stop point potentiometer. The generator will complete one cycle and stop when it returns to the point at which it started. In the gated mode the generator is initially OFF. When a triggering signal is applied at the front panel, the generator will generate an integer number of cycles dependent upon the width of the triggering signal applied at the front panel. The starting and the stopping point of the cycles generated is once again determined by the start-stop point potentiometer.

MANUAL TRIGGER BUTTON

The manual trigger button generates one cycle on command when the generator is in the triggered mode. NOTE: Trigger level control should be in its extreme clockwise or counter-clockwise rotation.

TRIGGER INPUT CONNECTOR

A BNC connector on the front panel that allows the triggering signal to be applied to the trigger circuits of the Model 112.

TRIGGER SLOPE/LEVEL CONTROL

The trigger slope switch allows the operator to select the negative portion or the positive portion of a triggering signal on which it is desired to trigger. The level control allows the operator to select the point on the slope of the triggering signal at which it is desired to trigger. In the gated mode of operation with a sine wave, triangle, etc., as a triggering source, the trigger level control can be adjusted so that the trigger fires at different points on the input triggering signal and the generator will generate a different number of pulses for the same applied frequency and amplitude.

START-STOP POINT CONTROL

The start-stop point control allows the starting point of the integrator to be varied through $\pm 90^{\circ}$ when in the triggered or gated mode. The start-stop point potentiometer will allow the starting point to go beyond the -90° position in the fully counter-clockwise rotation, and beyond the $+90^{\circ}$ starting point in the fully clockwise position. To start and stop at -90°, the control can be rotated fully counter-clockwise and then backed-off until the starting point is -90°. The same is true of the $+90^{\circ}$ position or rotation. This insures that in all frequency ranges the operator will be able to achieve a starting and stopping point of $\pm 90^{\circ}$. It should be noted that if a start-stop point of $+90^{\circ}$ is exceeded, the unit will free run.

MODELS 115 AND 115B, CONTROLS AND TERMINALS

The controls, inputs, and outputs of the Model 115 and Model 115B are identical to those discussed for the Model 112 and Model 112B with the following exceptions.

PHASE LOCK CONTINUOUS TRIGGERED MODE SWITCH

The Model 115 has all the capabilities of the Model 112 to include the triggered and gated mode of operation. When the mode switch is in the triggered mode, the generator can be operated either in triggered or gated as a separate switch allows selection of either the triggered or gated mode. When the mode switch is in the phase lock mode, the generator can be phase locked to an external signal applied to the input BNC connector on the front panel marked "Trigger/Phase Lock In." When in the phase lock mode, the trigger level control becomes the "Phase Adjust Control" allowing the phase of the generator signal to be varied from zero to 180° with respect to the signal applied at the front panel. The generator will frequency lock to the applied signal at the front panel and the phase of the generated signal can be varied with respect to the signal applied at the front panel.

TRIGGER PHASE LOCK SLOPE/LEVEL/PHASE CONTROL

In the triggered or gated mode of operation this control performs the same function as was discussed for the Model 112. When the mode switch is in the phase lock position, the slope switch should be placed in the minus slope position and the level control becomes the phase adjust control. In its extreme counter-clockwise rotation, the phase difference with respect to the applied signal at the front panel is zero degrees. In the extreme clockwise position of the phase adjust, the signal generated is 180° out of phase with respect to the signal applied at the front panel connector. Various degrees of phase difference are adjustable throughout this range. If it is desired for phase to be 180° to 360° with respect to the applied signal at the front panel, the out of phase power amplifier output on the front panel can be used or the selected differential output on the rear panel can be used; the phase of these output can be adjusted from 180° to 360° with respect to the signal applied at the front panel.

PHASE "UN-CAL" INDICATOR LIGHT

Although the Model 115 and Model 115B will remain frequency locked over the entire frequency decade, the phase adjust control is calibrated only for a limited range. If the generator is locking to a frequency of 5 KHz, the OFF X.3 X1 switch should be in the X1 position, the frequency Hz switch in the X1K position, the frequency vernier in the "cal" position, and the dial of the Model 115 at the "5" position for maximum calibrated accuracy of the phase adjust control. The frequency it is desired to be phase locked to can be applied to the input connector on the front panel and the dial rotated through its range until the phase "un-cal" lamp goes out. Continuing to rotate the dial beyond this position will result in it lighting again. For maximum calibration accuracy it is best to have the dial setting in the center of the range where the light is not lit. The phase adjust control can then be used to vary the phase of the output with respect to the applied signal at the front panel.

NOTE

The generator will still frequency lock to the applied signal even though the phase "un-cal" lamp is illuminated.

TRIGGER GATED SWITCH

The trigger gated switch on the Model 115 is concentric with the start-stop point potentiometer and performs the same function of selecting either the triggered or gated mode as discussed for the Model 112. The mode switch, however, must be in the triggered position for the trigger gated switch to be operative.

START-STOP POINT POTENTIOMETER

The start-stop point potentiometer performs the same function in the Model 115 and Model 115B as it did for the Model 112, and that is to select the starting and stopping point of the integrator in the triggered or gated mode. There is an added switch on the rear of the start-stop point potentiometer in the Model 115 and the Model 115B, however. When the start-stop point potentiometer is rotated to its most counter-clockwise rotation, a switch is thrown that places the instrument in the 90° phase lock "cal" mode. The phase control has no effect when the instrument is in the 90° "cal" position.

MODELS 116 and 116B, CONTROLS AND TERMINALS

The Models 116 and 116B controls and terminals are identical to the Models 115 and 115B controls and terminals with the following exception. The trigger gated switch in the Models 115 and 115B is replaced with the triggered cycle switch in the Models 116 and 116B. The external position of the triggered cycle switch in the Model 116 is identical to the gated position of the trigger gated switch with the Model 115. For phase lock operation, the triggered cycle switch should be in the one cycle position. In the triggered mode of operation of the Model 116, if it is desired to gate rather than trigger, the external position of the triggered cycle switch can be selected. If it is desired to generate one cycle, the one cycle position can be selected, and so on, up to 256 cycles. The Model 116 can be triggered either by an external trigger source or by depressing the manual trigger button and a discrete number of cycles generated depending on the setting of the triggered cycle switch. This makes a convenient tone burst generator without requiring an external source. The generator will produce an integer number of cycles as set by the triggered cycle switch.

SECTION II
SPECIFICATIONS AND TEST PROCEDURES

This section contains specifications for the WAVETEK instruments discussed in this handbook, and procedures for testing their accuracy. This table provides specifications for the Models 112, 112B, 115, 115B, 116 and 116B.

NOTE

Specifications apply 10% to 100% of maximum amplitude setting.

VERSATILITY

Waveforms

Sine ∿, square ⊓, triangle ∧, ramp ◿, and sync pulse.

Dynamic Frequency

0.0015 Hz to 1 MHz (10 min. to 1 μsec.).

NOTE: Dial is a high quality composition potentiometer allowing true continuously variable frequency control.

Ranges

X.01 = 0.005 Hz to 0.1 Hz

X.1 = 0.05 Hz to 1 Hz

X1 = 0.5 Hz to 10 Hz

X10 = 5 Hz to 100 Hz

X100 = 50 Hz to 1 KHz

X1K = 500 Hz to 1 KHz

X10K = 5 KHz to 100 KHz

X100K = 50 KHz to 1 MHz

Ranges (cont.)

X.003 = 0.0015 Hz to 0.03 Hz

X.03 = 0.015 Hz to 0.3 Hz

X.3 = 0.15 Hz to 3 Hz

X3 = 1.5 Hz to 30 Hz

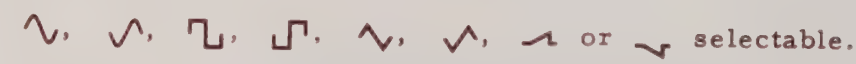
X30 = 15 Hz to 300 Hz

X300 = 150 Hz to 3 KHz

X3K = 1.5 KHz to 30 KHz

X30K = 15 KHz to 300 KHz

Nine Simultaneous Outputs

1)  selectable.

Amplitude adjustable over at least a 50:1 range.

Output impedance 50Ω (600Ω output impedance available by removing one jumper wire).

At least 30 volts peak to peak (15 volts ramp) into an open circuit.

At least 10 volts peak to peak (5 volts ramp) into a 50Ω load (the attenuator should be adjusted counter-clockwise until clipping stops).

Short circuit current ±100 ma.

"B" Models: A maximum of 5 volts peak to peak at 600Ω ±20% output impedance (2.5 volts ramp).

2) 50Ω 0.5 volt peak to peak, 10 nsec. risetime into 50Ω.

3) 50Ω 5 volts peak to peak, 15 nsec. risetime.

4) 50Ω 5 volts peak to peak.

5) 50Ω 5 volts peak to peak.

6) 50Ω 0 volts to -2.5 volts ramp; 50% duty cycle.

7) Sync pulse: At least -10 volts into an open circuit; less than 5 μsec duration.

8) High impedance 2.5 volts peak to peak offset +1.25 volts.

9) 50Ω , , , or selectable.

5 volts peak to peak differential output 180° out of phase with outputs 2 through 6.

NOTE: All outputs may be shorted without damage to the instrument.

Trigger

Input impedance is 10 KΩ.

Trigger mode: Manual or external voltage of ±0.5 volt will generate one cycle.

Gated mode: Discrete number of cycles may be generated by application of ±0.5 volt gate.

Up to 100 volts may be applied without damage to the input circuitry.

Trigger level and slope are adjustable by front panel controls. (These controls are similar to trigger adjustments of an oscilloscope.)

The start-stop point of the generated waveform is adjustable through 360° for frequencies of 0.0015 Hz to 100 KHz.

A sine squared waveform is available by adjusting trigger start control to the + or - 90° position and using the offset sine wave output number 8.

VCG - Voltage Controlled Generator

Over 20:1 frequency ratio (selectable in ranges of 3:1 allowing excellent range overlap). 4.75 volts input for 20:1 frequency ratio (0.5 volt ± 1% per Major dial division). Input inpedance 10KΩ.

Phase Lock - Models 115, 115B, 116, 116B only.

Frequency range is 10 Hz to 1 MHz.

Input impedance is 10 KΩ.

Input amplitude requirements are minimum 800 mv peak to peak to lock and 5 volts peak to peak sine wave for specified accuracy.

An input of 100 volts will not damage circuitry.

Unit will frequency lock to any input within 10 to 1 of the dial frequency and will be phase locked to the fundamental of the dial frequency within specified accuracy.

Phase accuracy is $\pm 10^{\circ}$ from 10 Hz to 10 KHz, $\pm 20^{\circ}$ from 10 KHz to 1 MHz.

Indicator "phase uncalibrated" light illuminates when selected phase relationship is exceeded. Unit will maintain frequency lock even when the light is on.

HORIZONTAL PRECISION

Dial Accuracy

±1% of full scale 0.0015 Hz to 100 KHz.

±2% of full scale 100 KHz to 1 MHz.

Electronic Frequency Vernier

One turn for approximately one minor dial division.

VCG Linearity

±0.1% frequency versus input voltage (frequency error 0.1% of total deviation - best straight line method). 0.0015 Hz to 100 KHz generated frequency. From 10% to 100% of maximum dial frequency.

VCG Bandwidth

100 KHz.

Frequency Stability

Short term: Drift less than ±0.05% of setting for 10 minutes.

Long term: Drift less than ±0.25% of setting for 24 hours.

No critical components requiring internal oven.

Jitter

±0.025% cycle to cycle stability.

VERTICAL PRECISION

Frequency Response

Amplitude change with frequency less than 0.1 db 0.0015 Hz to 10 KHz, 0.2 db 10 KHz to 100 KHz, 0.5 db 100 KHz to 1 MHz.

Peak to Peak Voltage Accuracy

±1% for 5-volt and 2.5-volt outputs.

±1% for 30-volt output into 600Ω at maximum gain.

±10% for 0.5-volt output.

Amplitude Stability

Short term: ±0.05% of maximum peak to peak values for 10 minutes.

Long term: ±0.25% of maximum peak to peak amplitude for 24 hours.

Symmetry

All waveforms, except ramp, are symmetrical about ground within ±1% of maximum peak to peak amplitude (external zero adjust rear-panel control provided for output number 1).

D-C Offset Stability

Short term: ±0.05% of maximum peak to peak amplitude for 10 minutes.

Long term: ±0.25% of maximum peak to peak amplitude for 24 hours.

PURITY

Sine Wave Distortion

Less than:	0.5%	0.0015Hz to 10KHz.
	1.0%	10KHz to 100KHz.
	2.0%	100KHz to 1MHz.
	3.0%	600KHz to 1MHz.

Induced distortion due to phase lock operation:

1%	10Hz to 100KHz.
2%	100KHz to 1MHz.

Triangle and Ramp Linearity

Greater than:	99%	0.0015Hz to 100KHz.
	95%	100KHz to 1MHz.

Ramp Fall Time

Less than 200nsec.

Square Wave Rise and Fall Time

0.5 volt output less than 10nsec. into 50Ω termination.

5 volt output less than 15nsec.

30 volt output less than 100nsec.

5 volt adjustable (battery models) less than 100nsec.

Total Aberrations

Less than 5% (overshoot, preshoot, etc.) when properly terminated.

Tilt

Less than 0.5%

Time Symmetry

All waveforms:	99%	0.0015 Hz to 100 KHz.
	98%	100 KHz to 1 MHz.

ENVIRONMENTAL

Temperature

All specifications listed except stability, are for 25°C ± 5°C.

For operation from 0°C to 55°C, derate all specifications by a factor of 2.

MECHANICAL

Dimensions

7-3/4 inches wide, 5-1/4 inches high, 11-1/2 inches deep

Weight

10 pounds net, 15 pounds shipping.

Color

Clear anodized aluminum.

Controls

OFF X.3-X1 power/dial multiplier switch, frequency range switch, frequency dial, frequency vernier, function selector switch, amplitude attenuator, d-c zero adjustment (rear), manual trigger, trigger level/slope, start-stop point, gated/continuous/trigger mode switch.

Power

Models 112, 115, 116:	105 volts to 125 volts or 200 volts to 250 volts, 50 Hz to 400 Hz. Less than 20 watts.

Power (cont.)

Models 112B, 115B 116B:	D-C rechargeable ni-cad batteries provided with built-in charger. Eight hours of operation on the batteries for every 16 hours of charge; simultaneous operation and charge.
	105 volts to 125 volts or 200 volts to 250 volts, 50 Hz to 400 Hz. Less than 30 watts.

NOTE

The covers of these instruments may be mounted flush with the front panel by removing the cover and replacing it using the alternate set of tapped holes in the spacer bars.

TEST PROCEDURES

GENERAL INFORMATION

Specifications apply only when the dial setting is between 0.5 and 10. Instruments should be within specifications within 30 minutes' warm-up time. All specifications are for 25°C ± 5°C and 105 to 125 volts a-c, 50 Hz to 400 Hz. All measurements must be made as described herein. Frequency stability specifications refer to constant temperature, line voltage, panel setting, and loads; testing must be made after one hour's warm-up at defined conditions.

TESTING INFORMATION

All frequency measurements should be made with the function selector switch on sine ∿, output attenuator set in the maximum counter-clockwise most position, all outputs disconnected (and VCG input disconnected) except the 10 nsec. square wave output which should be connected to a counter through a 50Ω cable using 50Ω termination at the counter. The frequency vernier should be within specifications for all combinations of the range switch and frequency dial.

Time symmetry measurements should be made using this setup and by measuring the positive and negative half cycles of the square wave. The two half cycle measurements should differ by no more than 2% of the total one cycle measurement for 99% symmetry.

Cycle to cycle jitter measurements should be made with this same setup. An oscilloscope with a delaying sweep or frequency counter may be used for cycle to cycle time jitter measurement.

VCG linearity should be made by again using the same setup as above, with the addition of a low impedance (50Ω maximum) source connected to the VCG input.

VCG input voltage should be measured with a high accuracy voltmeter such as the WAVETEK Model 201, 202 or equivalent.

OTHER KINDS OF TESTS

All voltage measurements should be made with an accurate wide band peak measuring device. It is strongly suggested that a Tektronix type W, or type Z plug-in with an appropriate oscilloscope be used for making these voltage measurements. The measuring device should have at least 50 KΩ input impedance and sufficient band width so that waveform peaks are accurately

measurable. The measurements sould be made individually with no loads connected to the instrument.

When making very accurate peak measurements, minor aberrations will be noted on the waveform due to the switching of the square wave. The peak value is that voltage that associates immediately prior to these minor aberrations. Accurate peak waveform measurements should be made at 1 KHz with the dial set at 10. Accurate high frequency measurements are difficult to make and require considerable care in lead connection, current, and cable termination.

Lack of symmetry is defined as the difference in the plus and minus peak voltages. For example: a 5 volt signal with 1% dis-symmetry could read +2.525 volts and -2.475 volts.

All fixed outputs should be measured individually with the function selector switch on sine ∿ , and the amplitude attenuator in maximum counter-clockwise position. The switch selectable output should be measured with the attenuator in maximum clockwise position and the appropriate function selected. Nothing should be connected to the binding posts when making this measurement.

When measuring the selectable output amplitude of the 112B, 115B and 116B, the measuring device should have at least 500 K input impedance. Sine distortion, triangle and ramp linearity, rise and fall time, total aberrations and tilt specifications should be made independently connecting only one output to the appropriate measuring device at a time.

BNC outputs (except sync) should be connected to the measuring device with a 50Ω cable properly terminated for making all high frequency measurements.

Sync output and selectable output should be evaluated using maximum attenuator setting commensurate with the load.

GENERAL NOTE

The Test Procedures very specifically define individually making measurements without simultaneous load of the various connectors. Simultaneous loading of all outputs will have only a minor effect on the frequency amplitude and purity performance.

SECTION III
THEORY OF OPERATION
Model 112

Figure 1 is a basic block diagram of a function generator capable of delivering triangle, square and sine wave outputs. A discussion of the basic block diagram leads to easier understanding of the Models 112, 114, 115 and 116.

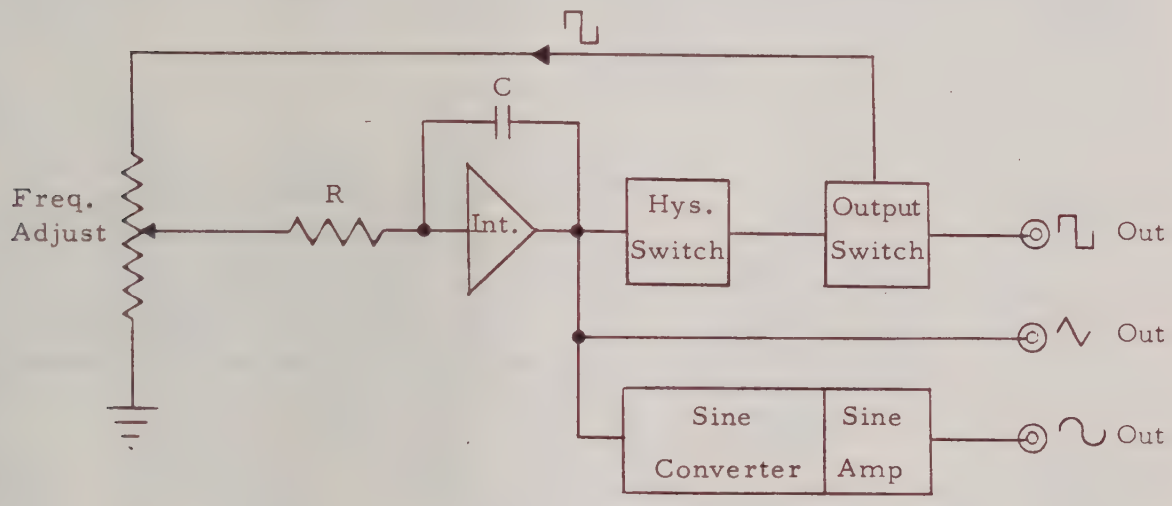


FIGURE 3-1

The heart of the basic function generator shown above in figure 1 is the integrator, a high gain, wide band d-c amplifier in an operational amplifier configuration connected for integration. Application of the negative half cycle of a square wave to resistor R results in a current directly proportional to the d-c level of the negative portion of the square wave and inversely proportional to the value of resistor R. The operational amplifier configuration offers a very high input impedance and most of the current in resistor R flows in and charges capacitor C. The right-hand side of capacitor C, and therefore the output point of the amplifier, is a positive going voltage slope. At a predetermined level, the positive going slope switches the bi-stable hysteresis switch which in turn switches the output switch, and the square wave switches to its positive half cycle. The current in resistor R changes direction and capacitor C charges in the opposite polarity. The output of the integrator is now a negative going voltage slope completing the triangle waveform. When the negative going slope reaches a predetermined level, it switches the hysteresis switch, which in turn switches the output switch, and the negative portion of the square wave is once again applied to resistor R. With the hysteresis switching levels fixed, the generated frequency is governed by the values of R and C and the amplitude of the applied square wave. With fixed values of R and C, varying

the amplitude of the square wave picked off and applied to the integrator by the frequency adjust pot (shown in figure 1) will vary the frequency. By changing either the value of R or C, the range of frequencies over which the unit will operate with the same frequency adjust pot can be changed. A square wave is available from the output switch and a triangle wave at the output of the integrator. The triangle wave is also fed into a converter which shapes it into a sine wave. Some attenuation is involved, therefore, a sine amplifier is added and a sine wave output is available.

The Model 112 uses analog control of frequency rather than the frequency pot shown in figure 1. Figure 2 is a basic block diagram of the Model 112, without the trigger mode.

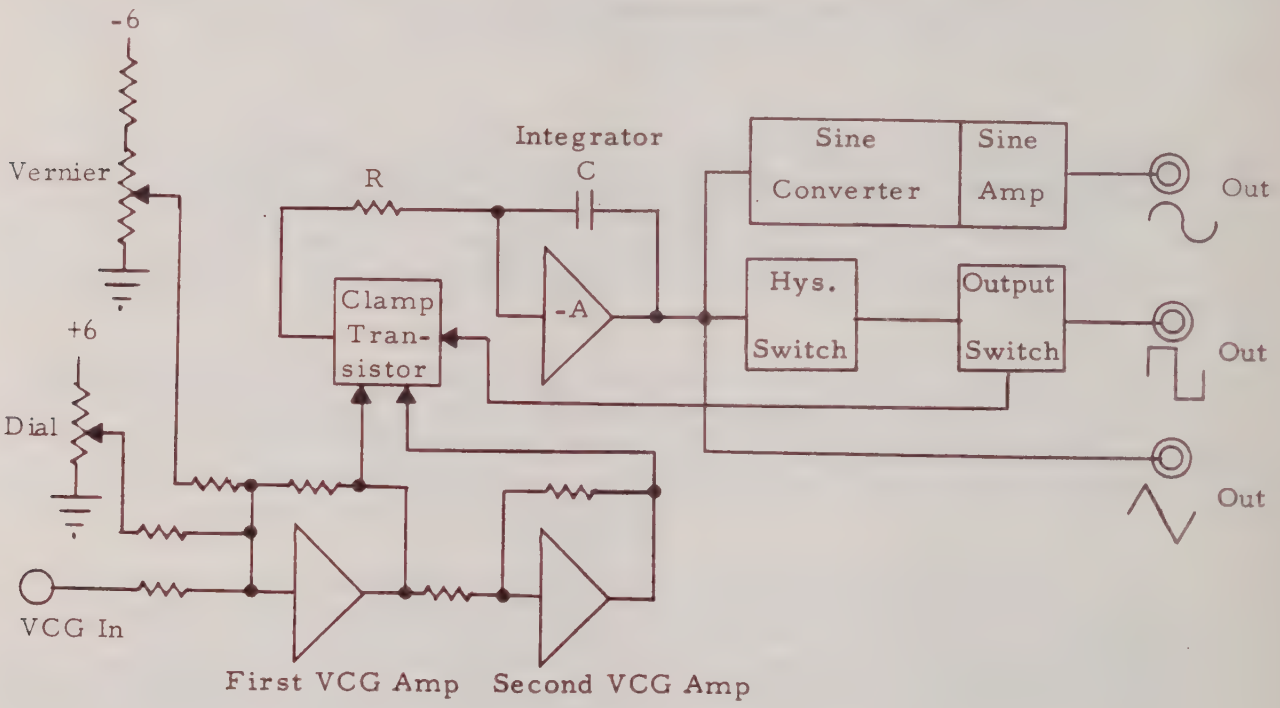


FIGURE 3-2

Basic operation is the same with the exception of frequency control. Changing the range over which the analog frequency control operates is done with the "Freq Hz" switch which changes the value of R or C, or both. The square wave is not applied to the integrator, but alternately turns on one of a pair of transistor clamps. The transistor clamps connect the output of two operational amplifiers alternately to the input of the integrator. The negative portion of the square wave turns on a clamp that connects the output of the first VCG amplifier to the integrator input. The positive portion of the square wave turns on a clamp that connects the output of the second VCG amplifier to the input of the integrator. The result is a square

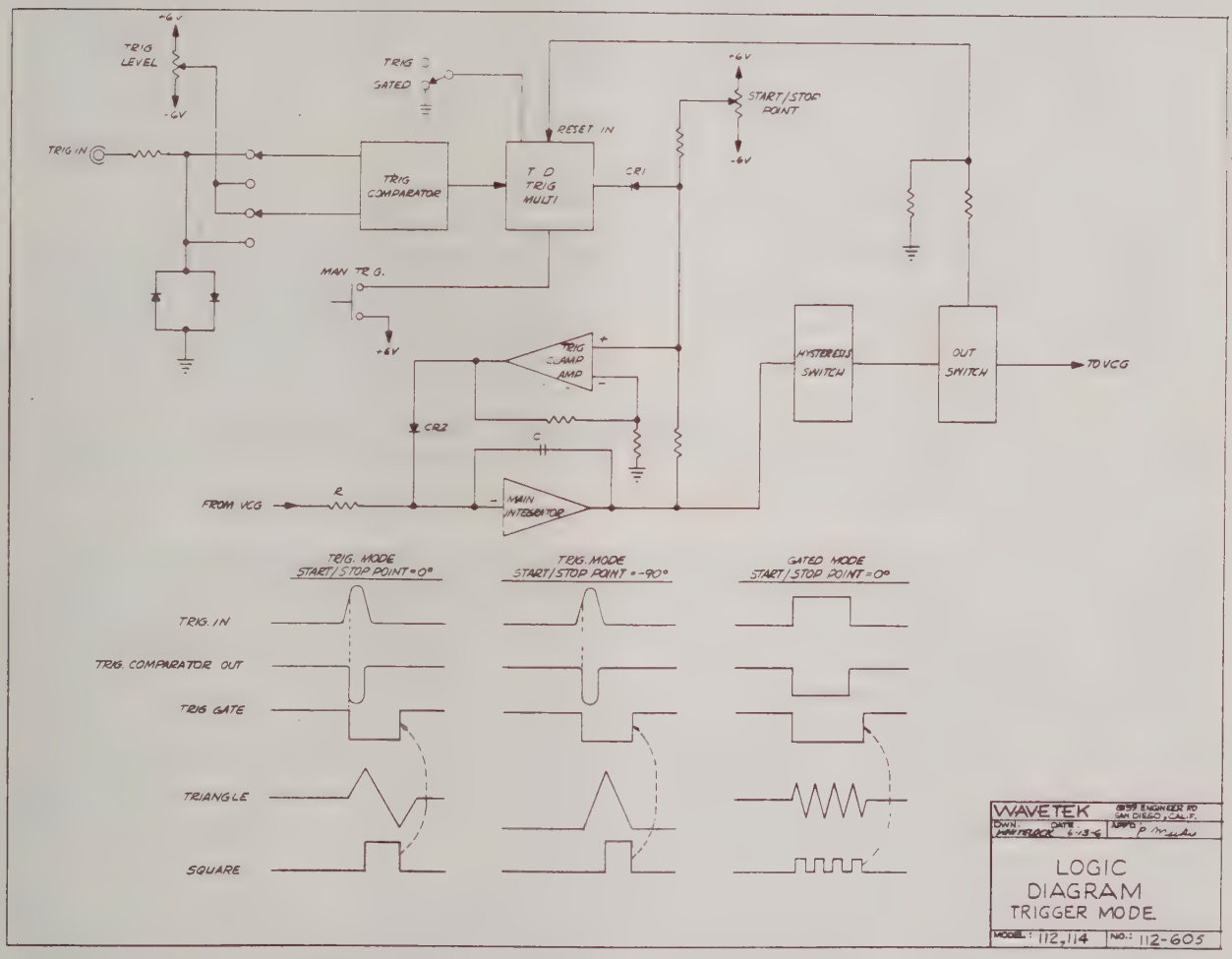

+6V
TRIG LEVEL
-6V
TRIG
GATED
RESET IN
+6V
START/STOP POINT
-6V
TRIG IN
TRIG COMPARATOR
T. D. TRIG MULTI
CR1
MAN TR G.
+6V
TRIG CLAMP AMP
HYSTERESIS SWITCH
OUT SWITCH
TO VCG
CR2
C
FROM VCG
R
MAIN INTEGRATOR
TRIG. MODE START/STOP POINT = 0°
TRIG. MODE START/STOP POINT = -90°
GATED MODE START/STOP POINT = 0°
TRIG. IN
TRIG. COMPARATOR OUT
TRIG GATE
TRIANGLE
SQUARE
WAVETEK
8559 ENGINEER RD SAN DIEGO, CALIF.
DWN. MAYERICK
DATE 6-13-6
APP'D P. Mayer
LOGIC DIAGRAM TRIGGER MODE
MODEL: 112,114
NO.: 112-605

Figure 3-3

wave applied to the integrator, the amplitude of which is determined by the levels at the outputs of the two VCG amplifiers.

The VCG amplifiers are similar d-c wide band amplifiers in inverting operational amplifier configurations. The first amplifier has a gain of approximately 3/5 and the second, a gain of unity. Applying +5 volts to the input of the first VCG amplifier results in a -3 volts at its output. This -3 volts is applied to the second VCG amplifier resulting in +3 volts at its output. The square wave under these conditions would operate the clamps and a ±3 volt square wave would be applied to the integrator. Since the VCG amplifiers are wide band, an a-c signal up to 100 KHz can be applied and the generator frequency modulated. The input summing node of the first VCG amplifier sums the dial input, the vernier input, and any voltage applied to the VCG input jacks. With no VCG input voltage applied, the dial and the vernier control the frequency.

Refer to the Block Diagram of Model 112.

The blocks on the left-hand side of the dial pot and frequency vernier in the diagram are concerned with triggered operation. The blocks on the right are similar to the blocks just discussed with the addition of an output power amplifier, a -1 amplifier, and an offset sine wave circuit.

The offset sine wave circuit adjusts the level of the sine wave available from the sine amplifier so that its most negative excursion is ground and its most positive excursion is +2.5 volts.

The -1 amplifier inverts the selected waveform and provides an inverted output to its BNC connector on the rear panel. When selected, the -1 amplifier also delivers the input to the output power amplifier through its attenuator allowing the power amplifier to deliver waveforms in phase or 180° out of phase with the waveforms available at the fixed output BNC connectors at the rear panel.

The output power amplifier is capable of delivering 30 volts peak to peak sine, square, and triangle waves into a 600Ω load, 10 volts peak to peak into a 50Ω load. It will also deliver a 15 volt peak ramp waveform into 600Ω, 5 volts peak into 50Ω.

The triangle wave is fed to the ramp circuitry where its d-c levels are adjusted so that the most positive excursion of the triangle is ground and the most negative excursion is -2.5 volts. The positive going portion of the triangle is then chopped to ground resulting in a -2.5 volt ramp, the phase corresponding to the negative going slope of the triangle wave.

The trigger circuitry and its switches are shown at the left in the diagram. Figure 3-3 is a simplified block of the triggered mode with waveforms. When the 112 is in the triggered mode and ready, the output of the tunnel diode trigger gate is near ground potential. CR1 in figure 3-3 is non-conducting and CR2 is on, clamping the output of the integrator at the level set by the start-stop point potentiometer,

through the trigger clamp amplifier. When a triggering signal is applied to the trigger input connector which overcomes the level set by the trigger level control, the tunnel diode trigger gate steps to approximately -6 volts turning on CR1. The output of the clamp amplifier is driven negative, disconnecting or turning off diode CR1 which allows the integrator to start. The d-c level at which it starts is set by the Start-Stop point potentiometer. The tunnel diode trigger gate is reset by the square wave from the output switch. Resetting the trigger gate enables the clamp amplifier once again; however, the triangle output must reach the Start-Stop level before the clamp amplifier takes control. This insures that the integrator output always starts and stops at the level set by the Start-Stop point potentiometer. The Start-Stop point potentiometer allows adjustment of ±90° to the starting and stopping point of the integrator. By using the output of the -1 amplifier (selected output) or by using the inverted output of the power amplifier, the Start-Stop point becomes adjustable over 360°. When the mode switch is in the gated position an integer number of cycles is generated governed by the width of the trigger pulse or gate applied to the trigger connector. When in the triggered position, one cycle is generated each time a triggering signal is applied or the manual trigger is depressed. Adjustment of the trigger level control when in the gated mode allows a limited range for changing the number of cycles for a given pulse width.

DETAILED CIRCUIT DESCRIPTION

Refer to Model 112 Main Board schematic diagram.

INTEGRATOR, MAIN BOARD

Q1 through Q10 and their associated circuitry make up the wide band d-c integrator amplifier. The "Freq Hz" switch on the front panel selects the appropriate integrating resistors and capacitors for frequency ranging.

Q1 and Q2 are a Darlington input pair for the minus input; Q 4 and Q 3 are a Darlington pair in the plus input. Transistors Q1 through Q4 are low current, high gain, wide band transistors which allow the inputs to operate with less than 40 nano amps of source current. The collectors of Q2 and Q3 work into a complex load made up of R1, R3, R4, C3, and the input impedance of Q5 and Q6. Q5 and Q6 form a differential amplifier stage driving the differential stage made up of Q7 and Q8. The output is taken off single ended at the collector of Q7 through the push-pull emitter follower, Q9 and Q10. CR1 and CR2 provide the bias voltage for Q9 and Q10 to prevent crossover distortion. R8 allows the d-c levels in the two sides of the amplifier to be balanced throughout. The triangle output is connected to pin 1. It is also fed through R22 to the sine converter and to the Hysteresis switch made up of Q25 through Q30.

HYSTERESIS AND OUTPUT SWITCH, MAIN BOARD

The transistors in the Hysteresis switch are connected to form a bi-stable switch. Either the Q25, Q26 side or the Q28, Q30 side can be on but not both at the same time. When the positive going triangle reaches the firing level set by R77, the

Q26 side turns on and the Q28 side turns off. The triangle starts its negative slope and when it reaches the firing level set by R78, the Q28 side turns on and the Q26 side turns off. The Hysteresis switch is d-c coupled to the bi-stable output switch made up of Q31 through Q34. The square wave available from this output switch has a risetime of less than 10 nano seconds. The square wave is coupled to pin 10.

The 10 volt peak to peak square wave is differentiated, amplified and clipped by Q35, R96, C25, CR15, R101, C27, and R110 to provide a -10 volt sync spike which has a duration of less than 5 μsec. The sync pulse is coupled to pin 13. The square wave is also coupled to a push-pull super emitter follower made up of Q36 through Q39. R104 allows the output amplitude to be adjusted, R99 adjusts the waveform so that it is symmetrical about ground. Diodes CR16 through CR19 provide temperature compensation. The output of the super emitter follower is a 5 volt peak to peak square wave with a risetime less than 15 nano seconds, coupled to pin 11.

SINE CONVERTER AND AMPLIFIER, MAIN BOARD

Transistors Q11 through Q18 are emitter followers in the sine converter that bias and temperature compensate the clipping diodes, CR3 through CR10. Diodes CR3, CR5, CR7, and CR9 clip the positive portion of the triangle at points set by the pots in the base of their associated emitter follower transistors. Diodes CR4, CR6, CR8, and CR10 clip the negative portion of the triangle. The diodes do not, however, clip the most positive and negative peaks of the triangle. Therefore, the input to the sine amplifier is a sine wave with small peaks at the top and bottom. The sine wave is fed to the plus input of the sine amplifier through R64. The sine amplifier is a d-c wide band operational amplifier connected in a potentiometric configuration. R69 is the feedback resistor. The peaks on the sine wave are also seen at the collectors of the emitter followers in the sine converter. These peaks are coupled through R54 and R56 to the minus input of the sine amplifier and peak cancellation occurs in the amplifier giving a clean sine wave at the output. The sine wave is coupled to pin 9. R60 adjusts the sine wave symmetry about ground and R64 adjusts the sine wave amplitude.

POWER SUPPLY AND OUTPUT AMPLIFIER BOARD (Refer to schematic diagram)

A-c voltage is coupled from the transformer to pins 14 and 15 to drive the bridge rectifier made up of diodes CR1 through CR4. Filtering is provided by C1 and C2. Q1 is a transistor connected and operated as a zener diode providing a reference voltage for the +6 volt supply. Q2 and Q3 make up a comparator type differential amplifier. Q2 and Q3 drive Q6 and Q7 which in turn drive the +6 volt pass transistor, Q10. R24 allows the base of Q3 to be adjusted slightly negative with respect to ground. Q1 has a zener voltage of approximately 6.3 volts setting the base of Q2 slightly negative. R24 is adjusted to give an output of +6.00 volts. If the +6.00 volts tries to increase due to a change in line voltage or load current, the collector of Q1 becomes more positive. The base of Q2 becomes less negative (moves in a positive direction with respect to ground) and Q2 draws more current. The collector

of Q2 moves less positive and this change is coupled through Q6 and Q7 to the base of Q10. This increases the resistance of Q10, returning the supply to +6.00 volts.

Q4 and Q5 form a comparator type differential amplifier in the -6.00 volt regulator. The base of Q4 is returned to ground through R6. The divider of R26 and R27 between the plus and minus 6 volt supplies sets the base of Q5 at ground. R9 allows a small adjustment of the currents in Q4 and Q5 to set the output at -6.00 volts. An increase in the -6 volts due to line voltage variation or load current variation, results in the base of Q5 moving negative. The collector of Q5 moves less negative (in a positive direction). This change is coupled to the bases of Q11 and Q12. Q11 and Q12 form a Darlington connected pass transistor pair for added gain. The positive going change, increases the resistance of Q11 and Q12, returning the output to -6.00 volts.

OUTPUT AMPLIFIER

Q13 through Q18 form an operational output amplifier with a gain of approximately -6 set by feedback resistor R37 and the input resistor made up of R31 and R32. Transistors Q13 and Q14 are a differential input stage driving a second differential stage of Q15 and Q16. The output is taken off single ended at the collector of Q16 and coupled to the push-pull emitter follower, Q17 and Q18. Diodes CR5 and CR6 provide bias for the push-pull emitter follower to prevent crossover distortion. The output is coupled through R50 and R51 to pin 3. The input is selected on the front panel and comes in on pin 5. C10 and C11 allow the amplifier to be high frequency compensated and are adjusted to give the best Gaussian response when a 1 MHz square wave is applied. A-c is coupled from the transformer to pins 1 and 2 and drives the bridge rectifier made up of diodes CR7 through CR10. The outputs of the bridge rectifier are filtered by C14 and C15 providing the supply voltages for the output amplifier. R41 is the d-c balance control allowing the output to be adjusted for symmetry about ground. R41 is a screwdriver adjustment available from the rear panel. D-C OFFSET MODIFICATION. To convert the d-c balance control, R41, to a d-c offset control, remove R40 and R42, 10K 1% and replace with 2K 5% carbon resistors. R41 will now serve as a d-c offset control allowing the power amplifier output to be offset approximately ±5 vdc. It should be remembered that using an offset control limits the available peak output signal. The output will deliver 100 ma into a short circuit and 32.5 volts peak to peak into an open circuit. When terminated in 600Ω, the amplifier will deliver 30 volts peak to peak. When terminated in 50Ω, the amplifier will deliver 10 volts peak to peak. When offset +5 vdc, the output when terminated in 600Ω is only capable of swinging +10 volts peak. When offset +5 vdc and terminated in 50Ω, the output is at its positive going limit point.

The input available on pin 5 and delivered to the power amplifier is coupled through an attenuator potentiometer on the front panel. The signal delivered to the attenuator pot is selected by the front panel function selector switch. In the "in phase" position of the selector switch, the signals are passed through a -1 amplifier prior to being delivered to the power amplifier; therefore, the output of the power amplifier is in phase with the fixed outputs available at the rear panel. In the "out of phase"

position of the function selector switch, the selected signals are delivered directly to the function potentiometer from the signal sources and the signals are inverted in the power amplifier resulting in an output that is out of phase with the fixed outputs at the rear panel. The function selector switch also selects the signal that is delivered to the -1 amplifier and available on the rear panel connector marked "Selected Output". The signal when selected and delivered to the selected BNC connector on the rear panel is identical to, but 180° out of phase with the other fixed outputs on the rear panel.

VCG BOARD

Refer to the VCG schematic. The two VCG amplifiers are similar operational inverting amplifier configurations. The basic operational amplifier is a μA702C integrated circuit. IC1 is the first inverting operational VCG amplifier, and serves as the main frequency control. The dial voltage from the front panel is available on pin 9 and applied through R6 to the summing node of the operational amplifier.

The voltage from the vernier potentiometer on the front panel is available on pin 8 and applied through R5 to the summing node of the operational amplifier. Any voltage applied to the front panel VCG input connector is applied to pin 4 through R8 and R7 to the summingnode of the operational amplifier. The resultant output is the sum of the input voltages.

In the case of the more complex Models 115 and 116, a phase lock voltage is present on pin 6, and coupled through the filter network made up of R1, R2, R3, C1 and C2 to the summing node of the operational amplifier.

R4 is not included on the VCG board in the other models. R8 allows a calibration of the effect of a VCG voltage applied on the front panel to the output frequency of the instrument. CR1 and CR2 provide protection in case of an overvoltage applied at the VCG input terminal.

R9, R10 and R11 provide a zero adjust network for the non-inverting input to the operational amplifier. R51, R52 and R53 provide source current for the input of the first amplifier allowing summing node zero adjustment. R12 and R13 are the feedback resistors in the first operational amplifier. R13 is adjusted for frequency calibration at the high end of the dial, while R9 is adjusted for frequency calibration at the low end of the dial.

Pin 7 is the output point of the operational amplifier and Q1 serves as an emitter follower to provide added current swing in the negative direction at the output of the first VCG amplifier. The output at the emitter of Q1 is coupled

through saturated transistor Q3 to the feedback resistor R13 and also to the input resistor of the second VCG amplifier made up of R14 and R15.

The square wave output from the output switch on the Main Board is available on pin 13, and applied through R17 to the base of Q2. When the square wave is negative Q2 is turned on and saturated and the output of the first VCG amplifier is coupled through Q2 to pin 7, the VCG out terminal.

When the square wave is positive, Q2 is turned off. Q2 and Q3 serve as inverted switches. Q2, operating as an inverted switch, has a very low saturation voltage; however, to compensate for this voltage, Q3 is placed in the feedback loop of the first operational amplifier. This also temperature compensates the first VCG amplifier.

The first operational amplifier has a gain of approximately 3/5 with respect to the dial input, while the second operational amplifier has a gain of unity. The output of the first VCG amplifier is coupled through R14 to R15 to the summing node of the first operational amplifier.

R25 serves as a feedback resistor in the second operational amplifier. Q4 and Q5 serve the same purpose in the second operational amplifier as Q2 and Q3 in the first. However, the output of the second operational amplifier is moving positive, therefore, NPN transistors are used.

When the square wave from pin 13 is positive, Q4 is turned on and saturated coupling the output of the second VCG amplifier to pin 7, the VCG out terminal. Therefore, the signal on pin 7 is a square wave whose frequency is determined by the switching rate of the output switch set on the Main Board and whose amplitude is dependent on the levels at the output of the two VCG amplifiers.

Since the second VCG amplifier has a unity gain, it will provide an output of opposite polarity but of the same magnitude as the output of the first VCG amplifier. The square wave on pin 7 is that square wave applied to the input of the integrator on the Main Board and in turn determines the frequency of the generator.

R46 and R24 serve as the zero adjust control for the second VCG amplifier. R14 allows adjustment of the symmetry at the high end of the dial, while R46 allows adjustment of the output frequency symmetry at the low end of the dial.

IC1 and IC2, the two integrated circuits, require a +12 volt supply. The positive high voltage supply from the power amplifier on the power supply and power amplifier board is coupled to pin 5 of the VCG board, on to the collector of Q6 and in turn, to pin 8 of both the integrated circuits.

Q6 is a transistor connected and operated as a 6 volt zener diode. The emitter of Q6 is returned to +6 volts; therefore, its collector will be 6 volts above this level or +12 volts with respect to ground. Q6 thus serves as the +12 volt regulating element for the supply for the integrated circuits. When properly calibrated the system is so well balanced that it cannot start when the machine is first turned on. The square wave output from the VCG clamp transistor on pin 7 drives the input to the integrator.

R22 is added to provide an initial unbalance to allow the integrator to start. Once the machine is running, resistors R18 and R28 offset this unbalance introduced by R22 and the system is once again balanced.

RAMP CIRCUIT

The triangle wave is available on pin 1 and is offset and attenuated by resistors R31, R32, R33, R34 and R35 so that its most positive excursion is zero volts d-c and its most negative excursion is -2.5 volts. Transistors Q7 and Q8 are turned on and saturated by the negative portion of the square wave applied to their bases through R37 and R38. When turned on, Q7 and Q8 chop the positive going portion of the offset triangle to ground. The result is a negative going 2.5 volt ramp in phase with the negative going portion of the triangle output. The ramp is delivered to pin 10 through two emitter followers, Q9 and Q10. The two opposing base to emitter voltages insure that the ramp starts at ground and the emitter followers temperature compensate each other.

TRIGGER BOARD (Refer to Trigger Board schematic)

Q1 and Q2 make up a comparator type amplifier with Q3 providing a constant current source. The divider of R2 and R4 provide the bias level for the base of Q3. When the front panel trigger slope switch is in the plus position, the triggering signal is fed via pin 12 through R9 to the base of Q2. The base of Q1 is returned to the trigger level control via pin 13. When a positive going input triggering signal overcomes the reference level established by the trigger level control in the base of Q1, the current of Q2 decreases allowing its collector to move in the negative direction. In the triggered mode pin 15 is open and Q5 is biased to saturation providing a current path for CR2, the tunnel diode.

Tunnel diode CR2 is quiescently biased in its low voltage state. A negative going excursion at the base of Q5 coupled through CR1 causes CR2 to switch to its high voltage state. Tunnel diode CR4 is quiescently biased in its low voltage state. When tunnel diode CR2 switches to its high voltage state, this change is coupled through C4 and results in CR4 switching to its high voltage state turning on transistor Q7. The output coupled to pin 10 is initially at ground potential.

When Q7 turns on, its collector moves in the positive direction and the output steps to approximately -6 volts. A reset pulse is coupled in through pin 21 through C5 to the base of Q6. This is a negative going reset pulse coincident with the negative going portion of the output square wave. This reset pulse results in the collector of Q6 moving positive and resetting the tunnel diode CR4 to its low voltage state. Transistor Q7 returns to its off state and the output returns to ground.

When the front panel mode switch is in the gated position, the base of Q5 is returned to ground by grounding pin 15. Transistor Q5 is turned off removing the current path for tunnel diode CR2. The triggering will now couple through CR1 and cause CR4 to switch to its high state; however, CR4 will remain in its high state until the triggering signal is removed. Therefore, the trigger gate will have a duration determined by the width of the trigger pulse applied at the input.

TRIGGER CLAMP AMPLIFIER

The trigger clamp amplifier is a d-c operational amplifier connected in a potentiometric configuration. Transistors Q10 and Q11 form an input differential pair driving the differential pair of Q12 and Q13. The collector of Q12 is returned to ground while the output is taken off single ended from the collector of Q13, which drives the push-pull emitter follower made up of Q14 and Q15.

CR7 and CR8 provide the bias for Q14 and Q15. R43 is the feedback resistor. R29 allows the amplifier to be d-c balanced so that the start-stop point potentiometer is adjustable between $\pm 90^{\circ}$ of the generated cycle. The output is taken off the junction of R40 and R41 to pin 3. In the trigger and gated mode, the output is coupled through a diode to the minus input of the main integrator. The output of the main integrator is coupled in on pin 7 through R38 to the base of Q11. The trigger gate is coupled through a diode to pin 6 and the base of Q11 as well.

The start-stop point potentiometer provides the reference level at pin 1 and, therefore, at the plus input of the trigger clamp amplifier. In the triggered or gated mode, the trigger gate is initally at ground potential allowing the start-stop point potentiometer to set the reference level at the plus input of the trigger clamp amplifier. This sets the level at the output of the trigger clamp amplifier and, therefore, clamps the minus input of the main integrator to the level set by the start-stop potentiometer through the diode from the output of the trigger clamp amplifier. R29 allows the trigger circuit to be balanced so that the start-stop point moves between - 90 and +90 degrees.

When a triggering signal is applied, the trigger gate steps to a -6 volts driving the plus input of the trigger clamp amplifier negative and essentially disconnecting or cutting off the diode to the minus input of the main integrator

allowing the integrator to start. When the trigger gate is reset, the trigger clamp amplifier is once again enabled; however, the triangle wave coupled in on pin 6 must overcome the reference level set by the start-stop poteniometer before the clamp amplifier will once again clamp the main integrator. This insures that an integer number of cycles are generated and that the start-stop point will always be set by the start-stop point potentiometer.

MINUS 1 AMPLIFIER

The -1 amplifier has two main functions: 1) to provide a differential or out of phase output with the fixed output at the rear panel, and 2) to allow the power amplifier to generate signals that are in phase or 180° out of phase with the fixed outputs on the rear panel. The start-stop point potentiometer only allows the start-stop point to be varied ±90°. By using the output from the -1 amplifier or the inverted output from the power amplifier, the start-stop point can be made to operate over 360° since the start-stop point is inverted as well as the signal.

The -1 amplifier is an operational inverting d-c amplifier with a gain of unity set by potentiometer R63. Q20 and Q21 form a differential input pair driving the differential pair of Q18 and Q19. The output is taken off single ended from the collector of Q18 through push-pull emitter follower Q16 and Q17. CR9 and CR10 provide the bias for the push-pull emitter follower to prevent crossover distortion. R63 and R64 make up the feedback resistor while R62 is the input resistor. C15 and C18 are to shape the frequency response characteristics of the amplifier. C12 places the plus input of the amplifier at signal ground. R48 allows the amplifier to be d-c balanced so that the signal is symmetrical about ground.

OFFSET SINE CIRCUIT

The output from the sine amplifier is coupled in on pin 18 where it is attenuated by R52 and R55. R53 and R54 returned to +6 volts, offsets the sine wave as well. R54 allows the amount of offset to be precisely adjusted. The output on pin 15 is an attenuated sine wave whose most negative excursion is ground and whose most positive excursion is +2.5 volts. This provides a convenient output on the rear panel for such application as sine-square testing.

PHASE LOCK AMPLIFIER

Since the phase lock amplifier applies only to the Models 115, 115B, 116 and 116B, its discussion will be taken up in that section which applys to those models. The phase lock amplifier is not included on the trigger board in the Models 112, 112B.

BATTERY REGULATOR BOARD

The battery regulator delivers plus and minus 6 volts dc to the Models 112B, 115B and 116B from a pack of 1.2 ampere-hour rechargeable Nickel Cadmium batteries. The +6 and -6 volt regulators are equivalent circuits and operate in the same manner as the ac regulators on the standard supply board. Q13 is the series pass transistor for the plus supply and Q21 is the series pass transistor for the minus supply. Q17 and Q25 act as zener references for the two supplies. R19, Q9 and CR9 make up the "starting" circuit. This assures that the supplies achieve full output when first turned ON. R27, Q14 and R42, Q22 provide "current limiting" circuit which engages when the voltage across R27 (or R42 for minus supply) reaches approximately 0.6 volts. Q14 (Q22 for minus supply) conducts and limits the current through the series pass transistor. This occurs at approximately 340ma.

Transistors Q1 through Q7 make up the charging circuit. The batteries are always being charged as long as SW1 is on and the line cord is plugged in an ac source. The transformer delivers center-tapped ac to pins 1 and 2. The ac is rectified by diodes CR1, CR2, CR3 and CR4 and filtered by C1 and C2, providing +24 and -24 volts dc. R10, R11, R14 and R15 sample the charging current through the batteries and provide forward bias to Q6 and Q7 through divider R8, R9, R13 and potentiometer R12. When potentiometer R12 is turned maximum counter-clockwise, the current through the current sampling resistors should be approximately 40ma to bias Q6 and Q7 on. When this occurs the current through Q1, Q2, Q3 and Q4 is reduced and an equilibrium charge rate is reached. Turning R12 fully clockwise adjusts the bias on Q6 and Q7 such that approximately 120ma of charge current is required for equilibrium. Charge rate is adjustable from the rear panel.

This method sampling the battery current provides an essentially constant charge rate regardless of load current. It also yields an overall negative temperature coefficient which is necessary for extended battery life.

When SW1 is in the OFF position, and the power cord is connected to an ac source, R6 and R18 provide a "trickle" charge of approximately 6ma. This maintains the batteries at full charge during idle periods.

Since there is no 30 volt output amplifier in the battery instruments, the attenuator wiper arm is connected to the output binding post through a 470Ω resistor. This provides a maximum output of 5 volts peak to peak at 600Ω output impedance (2.5 volts ramp).

FRONT PANEL BOARD

The Model 112 front panel board contains the trigger input connector, the trigger slope switch and trigger level control, the start-stop point ·

potentiometer, the mode switch, the function selector for the power amplifier and for the selected differential output on the rear panel, the VCG input connectors, the manual trigger button, the frequency vernier, the timing capacitors and resistors for the main integrator, the main frequency dial, and the power amplifier output connectors.

The output of the power amplifier is available on pin 30 and coupled through R47 and R48 to the front panel connector. C9 attenuates the very high frequencies to insure good high frequency performance. The parallel resistance of R47 and R48 in series with a pair of parallel 49.9Ω resistors on the power supply and output amplifier board make up the 50Ω output resistance of the power amplifier. The jumper around R46 is removed when a 600Ω output resistance is desired.

The fixed amplitude triangle, sine, square wave, and ramp are fed to the function selector switch via pins 1, 22, 25, and 26. The selected function is coupled by the function selector switch to pin 32 which returns to the input of the -1 amplifier. In the "in phase" position of the function selector, the power amplifier is driven by the output of the -1 amplifier coupled in on pin 31. Note that the function selector couples the output of the -1 amplifier to the attenuator R40, and its series resistor R41 in the "in phase" positions.

The center arm of the attenuator couples to pin 28 which is the input of the power amplifier. In the "out of phase" positions of the function selector, the fixed amplitude functions are fed directly to the power amplifier attenuator and on to the input of the power amplifier. Therefore, in the "in phase" position of the function selector, double inversion taken place; one inversion takes place in the -1 amplifier, and the second inversion takes place in the power amplifier.

With reference to the power amplifier output, only one inversion takes place in the "out of phase" position of the function selector and that is in the power amplifier itself. Note that the function selector switch, however, always delivers the selected function to the -1 amplifier so that the output at the rear panel is a signal 180° out of phase with the fixed outputs and is that function selected by the front panel function selector.

Wafers 1 and 2 of the frequency hertz switch select the appropriate integrating resistors and capacitors for the different frequency ranges. Wafer 3 selects the resistors to balance the source current in the plus side of the main integrator with different values of integrating resistors are selected in the minus input. Wafer 4 provides compensating resistors from the VCG output to ground so that the VCG clamp transistors always see the same loading.

The frequency dial attenuates the +6 volt supply and supplies an input voltage to the VCG amplifier. The VCG input connector provides an external

connector to apply voltages to the VCG to control frequency. R9 and C10 provide high frequency compensation. The manual trigger, when depressed, allows one cycle to be generated without an external triggering source required. The start-stop point potentiometer provides the reference level on the trigger clamp amplifier to determine the starting and stopping point of the integrator when in the triggered or gated mode. Diode CR3 and resistor R49 are between the trigger gate output and the plus input of the trigger clamp amplifier. The trigger slope switch selects that slope of the input triggering waveform it is desired to trigger on. The trigger level control provides a reference level for the opposite input to the trigger comparator so that different levels of triggering signals can be used. CR1 and CR2 insure that a high voltage applied to the trigger input connector will not destroy the trigger circuitry. The mode switch selects either triggered, gated, or continuous modes. The difference between the triggered and gated mode was discussed when pursuing the trigger board. In the continuous mode the generator operates like the conventional Model 111.

MOTHER BOARD

The mother board in the Model 112 provides the interconnections between the various boards used in the Model 112 and also contains the impedance determining resistors in series with the outputs. The outputs are connected from the rear of the mother board to the rear panel board and its connectors. The exception is the power amplifier output whose resistors are found on the front panel.

REAR PANEL BOARD

The rear panel board contains the eight BNC connectors for the eight fixed outputs. It also contains some high frequency compensating components for clean high frequency waveforms.

Refer to Model 115 Block Diagram.

The operation and circuit description described for the Model 112 applies to the Model 115 as well. Model 115 users should first read the Circuit Description section of the Model 112 before pursuing the Model 115 Circuit Description. The Model 115 has all of the characteristics, outputs, and capabilities of the Model 112 with the addition of the Phase Lock Mode. The block diagram of the Model 115 is similar to that of the Model 112 with the addition of the phase lock amplifier and the phase lock capacitors. The mode switch has three positions in the Model 115: phase lock, continuous, and triggered. If the gated mode is desired, a separate switch allows gated operation when the mode switch is in the triggered position. There is also a phase lock indicator light for phase lock operation that indicates when the generator is not properly phase locked. When the mode switch is in the phase lock mode, the trigger level control becomes the phase adjust allowing the output phase of the instrument to be adjusted from 0 to 180 degrees with respect to the signal being applied to the phase lock input BNC connector. The phase lock control becomes adjustable over 360° when the inverted selected output on the rear panel is used or the inverted power amplifier output is used. When in the phase lock mode, a calibrated 90° phase difference between the output and the applied signal can be obtained by rotating the start-stop potentiometer fully counter-clockwise into its detent position. This throws a switch mounted on the back of the start-stop point potentiometer that places the phase lock mode in a 90° "cal" position.

In the phase lock mode the phase multivibrator is triggered by the signal applied to the front panel BNC input connector. The phase lock multivibrator is reset by the square wave. This output is coupled to the phase lock amplifier. The signal delivered to the phase lock amplifier is the difference between the firing point on the input signal and the reset point governed by the output square wave. These pulses are passed through the phase lock amplifier which is a low pass operational amplifier. The output of the phase lock amplifier is an analog voltage proportional to the difference in the firing point governed by the input signal and the reset point governed by the output square wave. With no input to the phase lock amplifier from the phase control potentiometer, the phase lock circuit is calibrated so that the output of the generator would have a 90° phase difference with respect to the applied input signal. When the phase control is in the zero degree position, a narrow pulse is applied to the phase lock amplifier, integrated to provide an analog voltage, which is applied to the VCG input and adjusts the phase of the output signal from the generator to be in phase with the applied signal at the front panel. When the phase adjust control is in the 180° position, a wider pulse is applied to the phase lock amplifier resulting in a larger voltage applied to the VCG amplifier and the phase of the output frequency is adjusted to be 180° out of phase with the applied signal on the front panel.

The figure on the following page is a basic block diagram of the phase lock mode with waveforms.

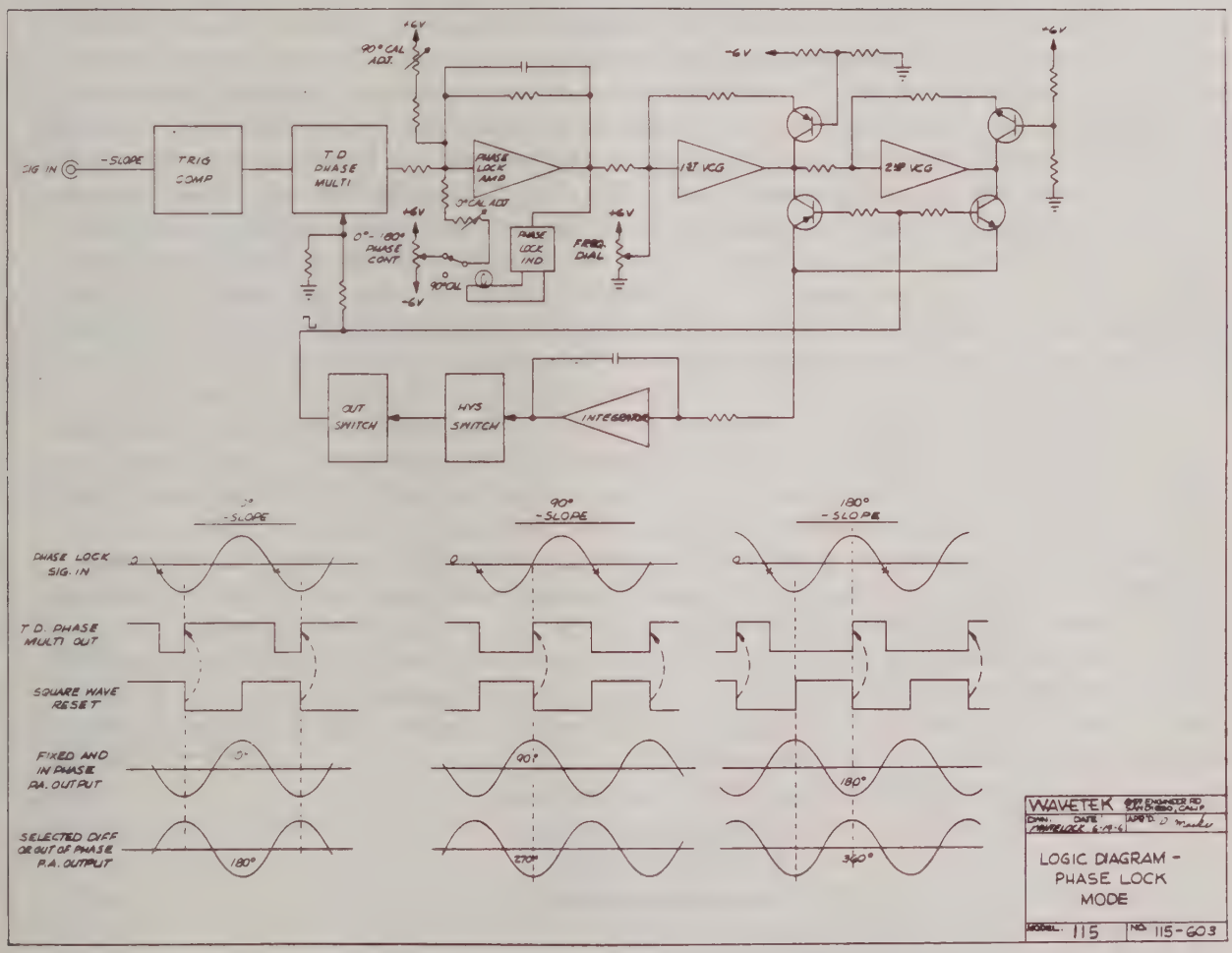

+6V
90° CAL ADJ.
-6V
+6V
SIG IN
-SLOPE
TRIG COMP
T.D. PHASE MULTI
PHASE LOCK AMP
1ST VCG
2ND VCG
3° CAL ADJ
0°-180° PHASE CONT
PHASE LOCK IND.
FREQ. DIAL
90° OSC
OUT SWITCH
HYS SWITCH
INTEGRATOR
3° -SLOPE
90° -SLOPE
180° -SLOPE
PHASE LOCK SIG. IN
T.D. PHASE MULTI OUT
SQUARE WAVE RESET
FIXED AND IN PHASE P.A. OUTPUT
SELECTED DIFF OR OUT OF PHASE P.A. OUTPUT
3°
90°
180°
270°
360°
WAVETEK
DWN
DATE
APP'D
PHASELOCK 6-19-6
LOGIC DIAGRAM - PHASE LOCK MODE
MODEL 115
NO. 115-603

Figure 3-4

For the greatest degree of accuracy the Model 115 should be operated in the phase lock mode with the trigger slope in the minus slopeposition. Note in the diagram that the minus slope of the applied phase lock signal in switches the tunnel diode phase multivibrator from 0 to approximately -6 volts. The negative going portion of the generated square wave resets the tunnel diode phase multivibrator. The output of the tunnel diode phase multivibrator is summed with the d-c level from the phase control and from the 90° "cal" adjustment at the minus input of the phase lock amplifier. The output is a d-c level established by the sum of the two voltages and the output of the tunnel diode phase multivibrator. The output of the phase lock amplifier drives the first VCG amplifier. The first VCG amplifier sums the input from the frequency dial, from the frequency vernier, and from the phase lock amplifier. Of course, it would also sum any applied voltage to the front panel VCG in connectors. In the 90° phase lock position of the start-stop point potentiometer, any input is removed from the 0 to 180 degrees phase control and the phase lock amplifier is automatically in the 90° phase lock condition. The waveforms on the left in the diagram show the conditions that exist when the Model 115 is in the phase lock mode with the phase control set at 0 degrees. The phase lock amplifier sums the voltage from the phase control and the output of the tunnel diode phase multivibrator. This establishes the phase of the output signal to be in phase with the applied signal at the front panel. This means, however, that the selected differential output on the rear panel and the out of phase power amplifier output are 180° out of phase with the signal applied to the front panel.

In the second set of diagrams the phase control is set at 90° and the output of the tunnel diode phase multivibrator is a symmetrical square wave. The phase of the output signal is now 90° with respect to the applied signal at the front panel referring to the fixed outputs and the in phase power amplifier output. The selected differential or out of phase power amplifier output is 270° with respect to the applied signal at the front panel. When the phase control is in the 180° position, the generated signal at the fixed outputs is 180° out of phase with respect to the signal at the input which sets a phase relationship with 360° for the output of the selected differential or out of phase power amplifier output with respect to the input signal. By adjusting the phase control and using the output that gives the desired phase difference, an output signal with a phase difference of 0 to 360 degrees can be obtained with respect to the input signal.

CAUTION

The trigger gated switch should be in the "triggered" position and the trigger slope switch should be in the minus slope position for calibration accuracy in the phase lock mode.

DETAILED CIRCUIT DESCRIPTION

TRIGGER BOARD

The Detailed Circuit Description of the trigger board covered in the Model 112 Circuit Description applies to the Model 115 as well with the exception that the Model 115 trigger board contains the phase lock amplifier. The phase lock amplifier is identical to the trigger clamp amplifier except that it is connected as an inverting operational amplifier rather than in a potentiometric configuration. The base of Q22 is the minus input. R73 is the 90° phase adjust and R81 is the 0° phase adjust. Pin 8 is connected to the trigger level/phase adjust control on the front panel in the phase lock mode. The output of the tunnel diode phase multivibrator is coupled in on pin 5 and applied through resistor R67 to the minus input of the phase lock amplifier in the phase lock mode. Phase lock capacitors are selected by the frequency hertz switch and connected between the phase lock amplifier output and pin 4, the minus input of the phase lock amplifier. Connections from the output of the phase lock amplifier to the VCG input are accomplished on the sub-panel.

POWER SUPPLY AND POWER AMPLIFIER BOARD, VCG BOARD, MAIN BOARD, and REAR PANEL BOARD Detailed Circuit Descriptions are discussed in the Model 112 Detailed Circuit Description section. These boards are interchangeable between the Model 112 and Model 115.

FIRST SUB-PANEL

The Model 115 first sub-panel contains the VCG input connector, the trigger input connector, the power amplifier output connectors, the manual trigger switch, the frequency dial potentiometer, the trigger slope switch, the trigger level control, the power amplifier function selector switch and output amplifier attenuator, the phase lock continuous trigger mode switch, and the phase lock "un-cal" indicator and its driving circuit. The triangle out, sine out, ramp out, and square wave output are available on pins 2, 21, 24, and 25 and delivered to the function selector switch. In the counter-clockwise position of the function selector switch (uppermost position in the diagram), the triangle is selected and delivered to the input of the -1 amplifier via pin 31. The output of the -1 amplifier is always available at the rear panel; therefore, on the first position of the switch, the triangle is delivered to the -1 amplifier, amplified by a factor of -1 and made available at the rear panel. The output of the -1 amplifier is also coupled in pin 30 of the front panel and delivered back to the function selector switch. In the counter-clockwise position of the function selector switch, the output of the -1 amplifier is delivered to the output amplifier attenuator and off the center arm of the attenuator to the input of the power amplifier via pin 27. In the first position of the function selector switch, the triangle receives a double inversion and is delivered to the front panel in phase with the fixed outputs on the rear panel. In the second position from the counter-clockwise position, the triangle is delivered directly to the attenuator and to the input of the power amplifier. Note that it is also still delivered to the input

of the -1 amplifier and, therefore, in both positions marked "triangle" of the function selector, an output will be delivered to the rear panel differential connector that is 180° out of phase with the triangle on the fixed connector on the rear panel. Similar switching occurs for the sine, ramp and square wave outputs.

The output of the power amplifier is delivered to pin 29 and to the GR connectors on the front panel. The manual trigger switch simply delivers a triggering signal to the trigger board when depressed and the generator will generate 1 cycle of the selected frequency. The start-stop point of the 1 cycle generated is determined by the start-stop point potentiometer setting. The dial potentiometer attenuates the +6 volts and delivers an input to the VCG via pin 16. R16 in series with the trigger in connector sets the input impedance of the trigger in circuitry. Diodes CR2 and CR3 insure that the trigger circuit will not be damaged if an overvoltage is applied at the trigger input connector. SW2, the trigger polarity switch, switches the inputs applied to the differential trigger amplifier on the trigger board so that the user can generate a triggering signal with a positive or negative going waveform. The trigger level adjust in the triggered mode provides a reference voltage on the opposite side of the differential trigger input circuitry than that connected to the trigger input connector and allows the point, on the applied waveform that triggering occurs, to be varied. When in the phase lock mode, the trigger level control is switched to the minus input of the phase lock amplifier and provide a variable voltage for adjusting the phase difference of the output signal generated by the unit and the applied phase lock signal on the trigger in connector. SW1, the mode switch, provides the logic switching for the three modes of operation of the Model 115. The uppermost pole on SW1 shown in the circuit diagram grounds the trigger amplifier input resistor in the plus input of the trigger amplifier in the phase lock and continuous mode and connects the output of the main integrator to the resistor at the plus input of the trigger amplifier in the triggered mode. The trigger gate is available on pin 13 and applied via the second pole to a resistor in the minus input of the phase lock amplifier when in the phase lock mode. The trigger gate is disconnected by the second pole in the continuous position and delivered to CR4 and CR5 and to the trigger amplifier plus input in the trigger mode. The third pole on the switch delivers the output of the phase lock amplifier to the phase lock indicator driver and also to the fifth pole on the switch when the switch is in the phase lock mode. The fourth pole on the mode switch delivers the output of the trigger amplifier via CR5 to the minus input of the main integrator when the switch is in the triggered mode. The fifth pole of the mode switch delivers the output of the phase lock amplifier to the phase lock VCG input via pin 12 when in the phase lock mode. In the continuous and triggered mode this pole grounds the phase lock VCG input. The final pole in the mode switch connects the trigger level adjust to the zero degree phase adjust potentiometer and on to the minus input of the phase lock amplifier when in the phase lock mode. In the continuous and triggered mode, the trigger level adjust is connected to the trigger input comparator circuit and serves as a trigger level control.

The phase lock "un-cal" driver circuit is a go/no-go configuration. The nominal level when in perfect phase lock is zero volts applied to the phase lock indicator driver. If the output of the phase lock amplifier swings sufficiently positive to turn on Q3, the collector of Q3 moves sufficiently negative to turn on transistor Q1 providing a current path for the phase lock "un-cal" light and the light is illuminated. The level required is approximately +0.6 volts. If the output of the phase lock amplifier moves sufficiently negative to turn on Q4, the collector of Q4 moves positive turning on Q2. The collector of Q2 moves negative turning on Q1 once again, providing a current path for the phase lock "un-cal" light. The Model 115 remains in frequency lock even though the phase lock "un-cal" light might be illuminated. The light turns on to indicate that the tolerances associated with the phase adjust control are being exceeded.

SECOND SUBPANEL

The second subpanel contains the phase lock capacitors, the frequency hertz switch and its associated frequency range capacitors and resistors, the start-stop point potentiometer and the 90° phase lock "cal" switch mounted on the rear of the start-stop point potentiometer, the main frequency vernier, and the trigger gated switch. Pin 14 connects to the phase amplifier output and pin 7 to the phase amplifier minus input placing R1 from the output of the phase lock amplifier to its minus input. The rear-most wafer of the frequency hertz switch selects the phase lock capacitor for that particular frequency range. The second pole from the left of the frequency hertz switch shown in the schematic diagram selects a resistor to ground for the VCG clamps driving the main integrating resistors. As a large resistor is selected as an integrating resistor, a resistor is connected to ground to provide a constant load on the VCG clamps. The third pole from the left in the schematic diagram on the frequency hertz switch selects resistors between the integrator balance potentiometer on the main board and the plus input of the integrator. As larger integrating resistors are selected, resistors are connected in the plus input of the main integrator to balance out the voltage developed by source current in the main integrator. The fourth pole from the left on the frequency hertz switch selects the integrating capacitor for frequency ranging. C1 is located on the front panel due to its size and is connected to the frequency hertz switch via pins 1 and 2 on the second subpanel. The fifth pole on the frequency hertz switch selects the appropriate integrating resistor for frequency ranging.

The "Off X.3 and X1" switch, SW2, allows different integrating resistors to be selected for the X.3 and X1 range to allow overlap between the range decade. The start-stop point potentiometer selects a dc voltage to be applied through resistor R30 to pin number 6 and on to the plus input of the trigger amplifier to determine the starting and stopping point of the main integrator when in the triggered mode. The 90° phase "cal" switch opens the line between the phase adjust on the front panel and the minus input of the phase lock amplifier when switched to the "90° cal" position (counter-clockwise

rotation of the start-stop point potentiometer).

The frequency vernier attenuates a portion of the -6 volt supply and delivers it to the input of the first VCG amplifier. The frequency vernier is in a "cal" position when it is in its most clockwise rotation. This grounds the vernier input to the first VCG amplifier. When rotated to its counter-clockwise position it supplies sufficient negative voltage to the first VCG amplifier to reduce the frequency approximately one minor dial division. The trigger gated switch, SW4, grounds pin 19 in the gated position to provide for gated operation on the trigger board. R35 and R36 attenuate the 10nsec. square wave available on pin 23 and deliver it to pin 24 which returns to the trigger reset on the trigger board. The level selected by the start-stop point potentiometer is available on pin 6, and delivered to the plus input of the trigger amplifier.

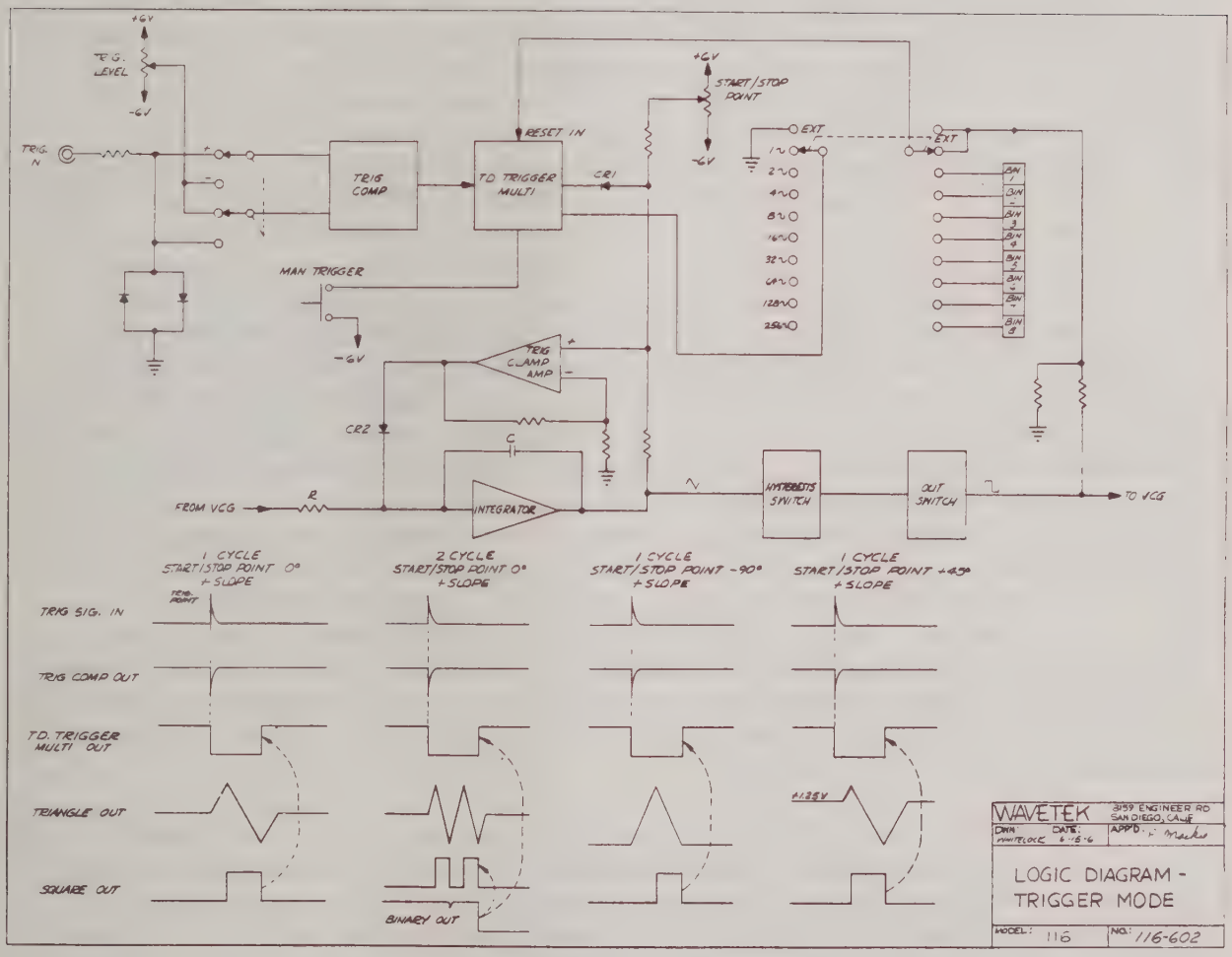

+6V
T.G. LEVEL
-6V
TRIG. IN
TRIG COMP
TD TRIGGER MULTI
RESET IN
CR1
START/STOP POINT
EXT
1 CYCLE
2 CYCLE
4 CYCLE
8 CYCLE
16 CYCLE
32 CYCLE
64 CYCLE
128 CYCLE
256 CYCLE
MAN TRIGGER
TRIG CLAMP AMP
CR2
C
R
FROM VCG
INTEGRATOR
HYSTERESIS SWITCH
OUT SWITCH
TO VCG
1 CYCLE START/STOP POINT 0° + SLOPE
2 CYCLE START/STOP POINT 0° + SLOPE
1 CYCLE START/STOP POINT -90° + SLOPE
1 CYCLE START/STOP POINT +45° + SLOPE
TRIG SIG. IN
TRIG COMP OUT
TD. TRIGGER MULTI OUT
TRIANGLE OUT
SQUARE OUT
BINARY OUT
+1.35V
WAVETEK
3159 ENGINEER RD SAN DIEGO, CALIF
DWN
DATE: 6-15-6
APP'D
LOGIC DIAGRAM - TRIGGER MODE
MODEL: 116
NO: 116-602

Figure 3-5

THEORY OF OPERATION
Model 116

Refer to Model 116 block diagram at the rear of the manual.

The Model 116 is basicly a Model 115 with an added built-in cycle counter. The Model 116 users should first review the circuit description of the Model 115 before studying the Model 116. All blocks in the Model 116 block diagram with the exception of those at the extreme left-hand side of the diagram, are the same as for the Model 115. The added circuitry in the Model 116 is a binary reset circuit, a power supply for the binarys used in the cycle counter, the cycle counter itself, and the switching involved. The binarys used in the cycle counter are integrated circuit J-K flip-flops and are used to count down the reset pulse applied to the trigger and phase tunnel diode multivibrator. Since the circuit description for trigger and phase lock modes of the Model 115 are the same for the Model 116, discussion of these will not be taken up in this section.

The external position of the triggered cycle switch is the same as the gated mode of operation for the Model 115. The one cycle position of the triggered cycle switch is the same as the triggered position of the Model 115. In the one cycle position, the reset pulse from the square wave output is fed directly into the trigger and phase tunnel diode multivibrator, and one cycle is generated on command by an externally applied triggering signal or by depressing the one cycle pushbutton on the front panel. In the two cycle position of the triggered cycle switch, the reset pulse from the square wave output is fed through on bistable multivitrator, an integrated J-K flip-flop, and therefore the instrument must go through two cycles of operation before the trigger multivibrator receives a reset pulse. The output of the first binary is coupled to the second binary and so forth through the eight binarys. In the four cycle position the reset pulse must pass through two binarys and, therefore, the instrument must go through four cycles of operation before a reset pulse is applied to the trigger circuit.

The use of the eight binarys to count down the reset pulse allows the Model 116 to generate 1, 2, 4, 8, 16, 32, 64, 128, and 256 discrete cycles for tone burst operation simply by selecting the number of cyles desired with the triggered cycle switch. The generator can be triggered either with an external triggering signal or by depressing the manual trigger button.

DETAILED CIRCUIT DESCRIPTION

Refer to the Model 116 Second Sub-Panel schematic at the rear of the manual.

The detailed circuit description as covered for the Model 115 applies to the Model 116 as well. The added circuitry on the second sub-panel to provide the

cycle counter will be discussed here. Detailed circuit description for the remainder of the Model 116 can be found in the section on detailed circuit description of the Model 115.

Q3 on the second sub-panel of the Model 116 serves as the pass transistor for an approximately 3.6 volt supply for the integrated flip-flop. The +6 volts is attenuated by R42 and R44 and applied to the base of Q3. The emitter of Q3 serves as the supply point for the binarys. Q4 is added to remove the supply voltage from the binarys in the external position of the triggered cycle switch. The base of Q4 is grounded in all positions of the triggered cycle switch by the second wafer and Q4 is non-conducting. In the external position of the triggered cycle switch, the ground at the base of Q4 is removed and Q4 comes into conduction grounding the base of Q3. This is added as a convenience for battery version users so that when not using the triggered or triggered cycle mode, the triggered cycle switch can be turned to the external position and conserve battery current since the binarys will be inoperative.

Transistors Q1 and Q2 and their associated circuitry adjust the phase and levels of the binary reset pulse to be compatible with the positive logic of the integrated binarys. The output of the tunnel diode trigger multivibrator on the trigger board adds levels of zero and -6 volts. These levels are available at pin 25 and applied to the base of Q2. In the zero state of the tunnel diode trigger multivibrator, the binarys are reset and inhibited. When the trigger gate goes to -6 volts, the binarys are enabled. When the input level at pin 25 is zero volts, the output at the collector of Q1 is approximately +3.6 volts applied to pin 7 of all of the binarys. This sets the quiescent state and inhibits the binarys. When the trigger gate steps to -6 volts, the level of the collector of Q1 moves to approximately zero volts and the binarys are enabled. Transistors Q5 and Q6 and their associated circuitry convert the positive logic output levels from the binarys back to the zero and -6 volt logic levels compatible with the Model 116. When a selected positive level from one of the binarys is supplied to the base of Q5, Q5 is turned on turning on Q6 and clamping the output delivered to pin 24 at ground. A zero level output in the selected binary has Q5 off, Q6 off and the output level delivered to pin 24 is -6 volts.

Section A of the triggered cycle switch selects the attenuated square wave in the external and one cycle position to be delivered to the trigger reset circuitry via pin 24. In the two cycle position it selects the output of the first binary to deliver the reset pulse, and so on. Section B of the triggered cycle switch grounds pin 19 in the external position and sets up the triggered circuitry on the trigger board in the gated mode, as was discussed with the Models 112 and 115. In the one cycle through 256 cycle positions, section B grounds the base of Q4 and divides the supply voltage for the integrated circuit flip-flops. When using a battery version of the Model 116 and not using the triggered cycle mode, it is desirable to place the triggered cycle switch in the external position to conserve battery current. When operating the Model 116 in the phase lock mode, the triggered cycle switch should be in the one cycle position.

The binarys are eight identical integrated circuits (J-K flip-flops). Pin 1 is the input point, pin 8 is the supply voltage, pin 7 is the pre-set or inhibit input, pin 6 is the output pin, pins 2 and 5 are connected together to set up the proper logic sequence, pins 3 and 4 are connected to ground.

SECTION IV
CALIBRATION
Model 112

MODEL 112 CALIBRATION PROCEDURE

EQUIPMENT REQUIRED:

1. Voltmeter, 1% accuracy, 1mv resolution (WAVETEK Model 201 or equivalent).

*2. Oscilloscope, Tektronix 530 Series or equivalent.

*3. Plug-in, Tektronix type W or equivalent.

4. Plug-in, Tektronix type CA or equivalent.

5. Frequency counter, 5 digit resolution.

6. Distortion analyzer Hewlett/Packard Model 330C or equivalent.

7. Two 50Ω cables with BNC connectors, 50Ω termination.

*If Tektronix scope and type W plug-in are not available, any peak reading device with an accuracy of 1% or better can be used.

Remove cover from instrument.

Set mode switch on continuous.

POWER SUPPLY BOARD

Bypass capacitors, C1 and C2, are located in the bottom of the instrument and are filter capacitors for the +6 volt and -6 volt power supplies. C2, the capacitor toward the rear of the instrument, is in the +6 volt supply, and the other is in the -6 volt supply. The capacitor leads are convenient voltage test points. Connect an appropriate measuring device between the end marked + of C2 and circuit ground. Adjust R24 for +6.00 volts ±1mv. Move the measuring device to C1 between the end marked - and circuit ground. Adjust R9 for -6.00 volts ±1mv. To compensate for the effects of interaction, repeat these adjustments.

There is no adjustment in the + and -24 volt supplies.

Typical 120 cycle ripple, ±6 volt supplies is less than 25mv.

Typical 120 cycle ripple, ±24 volt supplies is less than 500mv.

MAIN BOARD

1. Set range to X10KHz at top of frequency dial. Monitor the fixed triangle output and adjust R4 for minimum ringing on triangle. Set range to X100KHz and readjust R4 for linearity of the triangle at 1MHz. It may be necessary to repeat adjustments of R4 several times to insure optimum triangle linearity at 1MHz and minimum ringing at 100KHz.

2. Set range to X100 at extreme bottom of frequency dial. Use jumper to short pin 7, VCG board to circuit ground. Install 100K resistor between pin 1 and pin 3 of the main board. Observe integrator output with appropriate indicating device at junction of R17 and R18. Adjust R8 for zero volts. Remove jumper wire and 100K resistor.

3. Using Tektronix scope and type W plug-in, observe triangle at front panel connector, open circuit. Adjust R78 in switch set for the triangle break at exactly -2.50 volts (use comparison voltage on type W plug-in). Adjust R77 for the triangle break at exactly +2.50 volts. To compensate for effects of interaction, repeat adjustments.

4. Observe 15nsec. square wave for leading edge spikes with 50Ω cable terminated into 50Ω. Adjust R104 for + and -2.50 volts ±1mv. Adjust R99 for symmetry about ground. Tolerance on spikes is 5% of total peak to peak amplitude.

5. Observe that 10nsec. square wave output on oscilloscope is free of excessive leading edge spikes, (X100K, top of frequency dial, using 50Ω cable terminated into 50Ω).

POWER AMPLIFIER

Set output amplifier function selector (front panel) switch on square wave (fully clockwise position). Set attenuator fully clockwise. Observe front panel output GR connector on oscilloscope open circuited and adjust R31 for a 32.5 volt peak to peak square wave.

Adjust square wave with output attenuator fully counter-clockwise for symmetry about ground with R41. Adjust 1MHz square wave into open circuit with C11 for optimum square wave with no overshoot. Check for less than 100nsec. risetime. Check for 30 volts into 600Ω, and 10 volts into 50Ω.

SINE WAVEFORM ADJUSTMENTS

1. Using Tektronix scope and type W plug-in, set frequency dial at 10, range X100. Place main board on extender cable. Observe sine at BNC connector.

Adjust R64 for sine wave out of ±2.5 volts ±1mv. Adjust R60 for sine

symmetry about ground. Using distortion analyzer, adjust R20, R24, R30, R33, R46 and R49 for minimum harmonic distortion. Readjust R64 and R60 for amplitude and symmetry about ground. Typical harmonic distortion 0.12%.

2. Set dial at 1. Measure distortion. Typical distortion is 0.2%.

VCG BOARD
(For instruments having first amplifier summing node zero adjustment.)

Measure ±6 volt power supplies (refer to Power Supply Board Calibration Procedure, page 4-1).

1. Dial Setting Adjustment:

With Frequency Hertz switch at X100, Frequency Vernier fully clockwise, set Frequency Dial to 10, measure voltage at potentiometer wiper arm (pin 9 on the VCG Board) to be +5.750 volts ±2mv. If this condition is not met, re-install the dial.

2. Dial Tracking Adjustment:

With Frequency Hertz switch X100, Vernier fully clockwise, set dial to 10 and adjust R13 for 1000Hz and R14 for time symmetry. Set the dial to 1. By alternately shorting and opening the VCG input terminals, adjust R9 for a minimum frequency shift.

NOTE

Frequency shift is caused by non-zero summing node at the first VCG amplifier. R9 is used to adjust this for zero volts and no frequency shift.

Adjust R51 (source current potentiometer) and R46 for 100Hz and time symmetry. Repeat steps for adjustment of R13 and R14 and adjustment of R9 until frequency, symmetry and source current are all calibrated at the top (1000Hz) and bottom (100Hz) of the dial.

3. VCG Input Calibration:

With Frequency Hertz switch X100, Frequency Vernier Potentiometer fully clockwise, adjust dial for 100Hz on frequency measuring device. Apply +4.500 volts to the VCG input on the front panel and adjust R8 for 1000Hz.

4. Ramp Adjustment:

Observe ramp output at BNC connector with 50Ω cable unterminated. Adjust

R34 so that signal is neither nor , but is

Adjust R33 for -2.5 volts peak ramp output.

CHECK RANGES

On Front Panel Board check all fixed ranges for frequency tracking. Trim resistors have been installed on individual ranges for tracking. Adjust C3 for proper tracking on X10K range. A trim resistor has been installed between position 3 and position 5 on wafer 1 of range switch for proper tracking on X1K range. Adjust C7 for proper tracking on X100K range.

TRIGGER BOARD

Minus 1 Amplifier. Set "Freq Hz" X100, dial 10, mode switch continuous. Observe selected differential output with 50Ω cable unterminated with an oscilloscope with type W plug-in. Place function selector on front panel in position. Adjust R63, -1 amplifier gain control for 5.00 volts peak to peak. Adjust R48 for symmetry about ground. Rotate function selector through all positions and check for appropriate output waveforms.

Offset Sine. Observe offset sine output connector, open circuited with oscilloscope and type W plug-in. Adjust R54 for 2.5 volts peak to peak sine wave with the most negative excursion at 0.00 volts dc.

Trigger Clamp Amplifier. Set "Freq Hz" switch X100, dial at 10, mode switch triggered, Start-Stop Point centered, trigger slope +, trigger level centered. Apply 1 volt sine wave to trigger input. Adjust trigger level control for one cycle triggered operation. Adjust R29 so that Start-Stop Point Potentiometer will cause the observed waveform to shift beyond $\pm 90^{\circ}$.

Set mode switch to gated. Adjust trigger level to give several cycles. Switch slope switch between + and - and insure that gated operation is maintained.

Set mode switch to triggered. With triggering signal applied, adjust trigger level for 1 cycle triggering. Remove trigger signal source and depress manual trigger button. Observe 1 cycle when button is depressed.

FRONT PANEL OUTPUT

Observe power amplifier output with externally triggered scope. Rotate function selector through its positions and insure that all outputs are available and in proper phase.

MODEL 115/116 CALIBRATION PROCEDURE

EQUIPMENT REQUIRED:

1. Voltmeter, 1% accuracy, 1mv resolution (WAVETEK Model 201 or equivalent).

*2. Oscilloscope, Tektronix 530 Series or equivalent.

*3. Plug-in, Tektronix type W or equivalent.

4. Plug-in, Tektronix type CA or equivalent.

5. Frequency counter, 5 digit resolution.

6. Distortion analyzer Hewlett/Packard Model 330C or equivalent.

7. Two 50Ω cables with BNC connectors, 50Ω termination.

8. WAVETEK Model 110 or equivalent.

9. CMC-27D Frequency Counter, or equivalent (dual trace oscilloscope with delayed sweep and external input capabilities can be used in lieu of the CMC Counter).

*If Tektronix scope and type W plug-in are not available, any peak reading device with an accuracy of 1% or better can be used.

Remove cover from instrument.

Set mode switch on continuous.

POWER SUPPLY BOARD

Bypass capacitors, C1 and C2, located in the bottom of the instrument, are filter capacitors for the +6 volt and -6 volt power supplies. C2, the capacitor toward the rear of the instrument, is in the +6 volt supply, and the other is in the -6 volt supply. The capacitor leads are convenient voltage test points. Connect an appropriate measuring device between the end marked + of C2 and circuit ground. Adjust R24 for +6.00* volts ±1mv. Move the measuring device to C1 between the end marked - and circuit ground. Adjust R9 for -6.00* volts ±1mv. To compensate for the effects of interaction, repeat these adjustments.

*Adjust to 6.01 volts in Model 116B only.

There is no adjustment in the + and - 24 volt supplies.

Typical 120 cycle ripple, ±6 volt supplies is less than 25mv.

Typical 120 cycle ripple, ±24 volt supplies is less than 500mv.

MAIN BOARD

1. Set range to X10KHz at top of frequency dial. Monitor the fixed triangle output and adjust R4 for minimum ringing on triangle. Set range to X100KHz and readjust R4 for linearity of the triangle at 1MHz. It may be necessary to repeat adjustments of R4 several times to insure optimum triangle linearity at 1MHz and minimum ringing at 100KHz.

2. Set range to X100 at extreme bottom of frequency dial. Use jumper to short pin 7, VCG board to circuit ground. Install 100K resistor between pin 1 and pin 3 of the main board. Observe integrator output with appropriate indicating device at junction of R17 and R18. Adjust R8 for zero volts. Remove jumper wire and 100K resistor.

3. Using Tektronix scope and type W plug-in, observe triangle at front panel connector, open circuit. Adjust R78 in switch set for the triangle break at exactly -2.50 volts (use comparison voltage on type W plug-in). Adjust R77 for the triangle break at exactly +2.50 volts. To compensate for effects of interaction, repeat adjustments.

4. Observe 15nsec. square wave for leading edge spikes with 50Ω cable terminated into 50Ω. Adjust R104 for + and -2.5 volts ±1mv. Adjust R99 for symmetry about ground. Tolerance on spikes is 5% of total peak to peak amplitude.

5. Observe that 10nsec. square wave output on oscilloscope is free of excessive leading edge spikes, (X100K top of frequency dial, using 50Ω cable terminated into 50Ω).

POWER AMPLIFIER

Set output amplifier function selector (front panel) switch on square wave (fully clockwise position). Set attenuator fully clockwise. Observe front panel output GR connector on oscilloscope open circuited and adjust R31 for a 32.5 volt peak to peak square wave.

Adjust square wave with output attenuator fully counter-clockwise for symmetry about ground with R41. Adjust 1MHz square wave into open circuit with C11 for optimum square wave with no overshoot. Check for less than 100nsec. risetime. Check for 30 volts into 600Ω, and 10 volts into 50Ω.

SINE WAVEFORM ADJUSTMENTS

1. Using Tektronix scope and type W plug-in, set frequency dial at 10, range X100. Place main board on extender cable. Observe sine at BNC connector.

Adjust R64 for sine wave out of ±2.5 volts ±1mv. Adjust R60 for sine symmetry about ground. Using distortion analyzer, adjust R20, R24, R30, R33, R46 and R49 for minimum harmonic distortion. Readjust R64 and R60 for amplitude and symmetry about ground.

2. Set dial at 1. Measure distortion.

VCG BOARD
(For instruments having first amplifier summing node zero adjustment.)

Measure ±6 volt power supplies (refer to Power Supply Board Calibration Procedure, page 4-1).

1. Dial Setting Adjustment:

With Frequency Hertz switch at X100, Frequency Vernier fully clockwise, set Frequency Dial to 10, measure voltage at potentiometer wiper arm (pin 9 on the VCG Board) to be +5.750 volts ±2mv. If this condition is not met, reinstall the dial.

2. Dial Tracking Adjustment:

With Frequency Hertz switch X100, Vernier fully clockwise, set dial to 10 and adjust R13 for 1000Hz and R14 for time symmetry. Set the dial to 1. By alternately shorting and opening the VCG input terminals, adjust R9 for a minimum frequency shift.

NOTE

Frequency shift is caused by non-zero summing node at the first VCG amplifier. R9 is used to adjust this for zero volts and no frequency shift.

Adjust R51 (source current potentiometer) and R46 for 100Hz and time symmetry. Repeat steps for adjustment of R13 and R14 and adjustment of R9 until frequency, symmetry and source current are all calibrated at the top (1000Hz) and bottom (100Hz) of the dial.

3. VCG Input Calibration:

With Frequency Hertz switch X100, Frequency Vernier Potentiometer fully

clockwise, adjust dial for 100Hz on frequency measuring device. Apply +4.500 volts to the VCG input on the front panel and adjust R8 for 1000Hz.

4. Ramp Adjustment:

Observe ramp output at BNC connector with 50Ω cable unterminated. Adjust R34 so that signal is neither nor , but is .

Adjust R33 for -2.5 volts peak ramp output.

CHECK RANGES

Check all fixed ranges for frequency tracking. Trim resistors have been installed on individual ranges for tracking. Adjust C5 for proper tracking on X10K range. A trim resistor has been installed between position 3 and position 5 on wafer 1 of range switch for proper tracking on X1K range. Adjust C1 for proper tracking on X100K.

TRIGGER BOARD

Minus 1 Amplifier. Set "Freq Hz" X100, dial 10, mode switch continuous. Observe selected differential output unterminated with an oscilloscope with Type W plug-in. Place function selector on front panel in position. Adjust R63, -1 amplifier gain control for 5.00 volts peak to peak. Adjust R48 for symmetry about ground. Rotate function selector through all positions and check for appropriate output waveforms.

Offset Sine. Observe offset sine output connector, open circuited with oscilloscope and type W plug-in. Adjust R54 for 2.5 volts peak to peak sine wave with the most negative excursion at 0.00 volts dc.

Trigger Clamp Amplifier. Set "Freq Hz" switch X100, dial at 10, mode switch triggered, start-stop point centered, trigger slope +, trigger level centered. Model 115 trigger gated switch to "trig" (Model 116, "trig cycle" switch to one cycle). Apply 1 volt sine wave to trigger input. Adjust trigger level control for one cycle triggered operation. Adjust R29 so that start-stop point potentiometer will cause the observed waveform to shift beyond $\pm 90^{\circ}$.

Set Model 115 trigger/gated switch (Model 116, triggered cycle switch to external) to gated. Adjust trigger level to give several cycles. Switch slope switch between + and - and insure that gated operation is maintained.

Set Model 115 trigger/gated switch to triggered. With triggering signal applied, adjust trigger level for one cycle triggering. Remove trigger signal

source and depress manual trigger button. Observe one cycle when button is depressed.

Model 116 only: With a triggering signal applied, rotate the triggered cycles switch through all its positions and insure that the correct number of cycles are generated in each position.

FRONT PANEL OUTPUT

Observe power amplifier output with externally triggered scope. Rotate function selector through its positions and insure that all outputs are available and in proper phase.

PHASE LOCK CALIBRATION

NOTE

Insure that Model 115 trigger/gated switch is in the "trig" position or the Model 116 triggered cycles switch is in the one cycle position.

Set the Model 115 or Model 116 "Freq Hz" switch at X1K, mode switch phase lock, trigger slope minus, trigger level 90°, dial 5. Set the Model 110 function generator frequency hertz switch to X1K, dial at 5. Connect the 5 volt peak to peak sine wave from the Model 110 function generator to the in connector on the front panel of the Model 115/116. Connect the sine output of the Model 110 to one trace of a dual trace oscilloscope. Connect the sine output of the Model 115/116 to the other trace of the dual trace oscilloscope. Place the oscilloscope in the external trigger position and connect the Model 110 sync pulse to the trigger in connector on the oscilloscope. The two observed sygnals should be the same frequency with an adjustable phase difference that may be varied with the phase control on the Model 115/116 (trigger level control). The phase lock "un-cal" lamp on the Model 115/116 should be extinguished. Rotate the start-stop point potentiometer fully counter-clockwise until it is in its detent position. This is the 90° "cal" position for phase lock. A switch on the back of the start-stop point potentiometer places the instrument in the 90° "cal" position.

Connect the 10nsec. square wave output from the Model 110 to the "A" input connector of the CMC counter. Connect the Model 115/116 10nsec. square wave output to the "B" input of the CMC counter. Set the CMC counter to read time A to B. Set both the A slope and B slope on the CMC counter plus slope. Measure the time difference between the two 10nsec. square waves. This time difference should be 50 micro-seconds. Switch A slope and B slope on the CMC counter to minus slope. This reading should also be 50 micro-seconds. Adjust R73 for equal times when the CMC is on A and B

slopes positive and A and B slopes negative.

NOTE

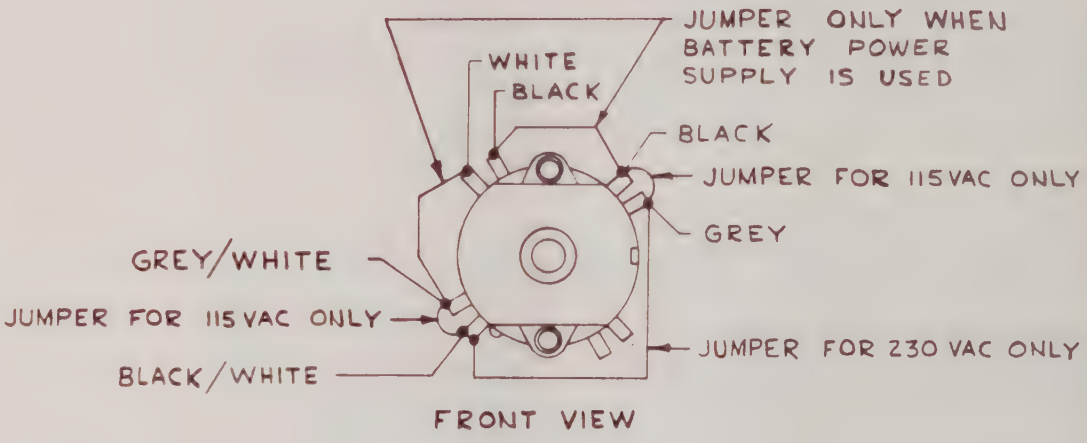
This measurement and adjustment is dependent upon the calibrated symmetry of the Model 110 and the Model 115/116 waveforms. It should be insured that the Model 110 is in calibration before attempting to use it to set the 90° "cal" position.

Rotate the phase lock 90° "cal" switch out of its detent position (start-stop point potentiometer). Adjust the trigger level/phase control potentiometer to the maximum counter-clockwise (zero degrees) position. Set the A slope and B slope switches on the CMC counter both to plus, CMC counter read time A to B. Adjust R81 for zero time between A and B. This means that the two signals have a zero degree phase difference.

Slowly rotate the frequency dial on the Model 115/116 in a counter-clockwise direction until the phase "un-cal" lamp is illuminated. The dial should read approximately 3.5. Slowly turn the Model 115/116 dial clockwise until the lamp extinguishes and just begins to light again. The dial should read now approximately 6.5 (insure that phase lock is maintained throughout this check). Slowly rotate the Model 110 dial through its entire range (if the Model 115/116 goes out of phase lock, the phase adjust/trigger level adjust/ control can be used to bring it back into phase lock). The instrument should phase lock to all frequencies throughout the Model 110 dial. Check the phase "un-cal" lamp and phase lock through the entire range on X10, X100, X10K and X100K ranges setting both the Model 110 and Model 115/116 frequency switches.

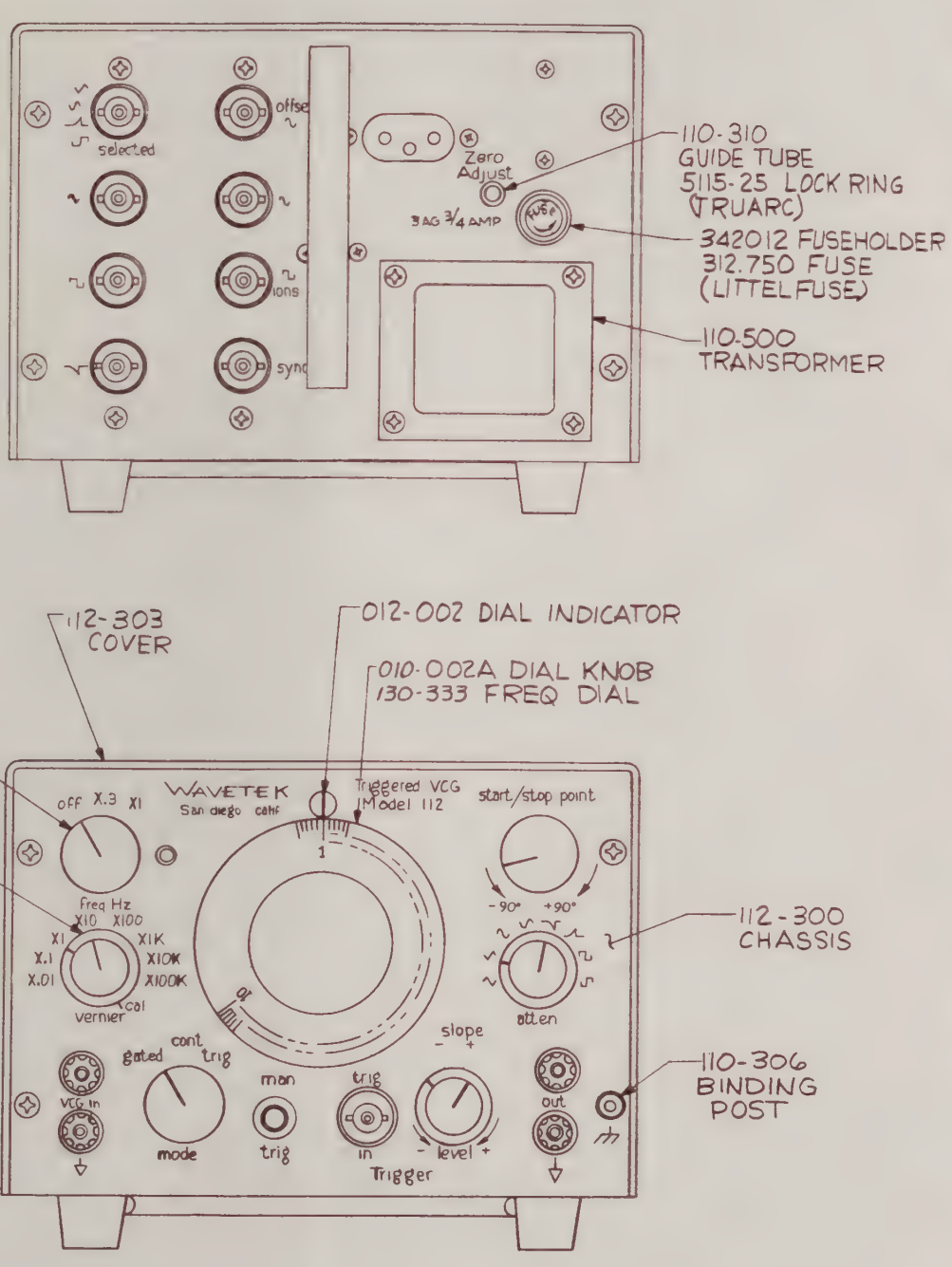
Connect the Model 115/116 sine output connector to a distortion analyzer. With the Model 115/116 phase locked to the Model 110 on frequency hertz X1K, dial 1, measure the sine distortion. The sine distortion should be less than 1.5% insuring that introduced distortion is less than 1%.

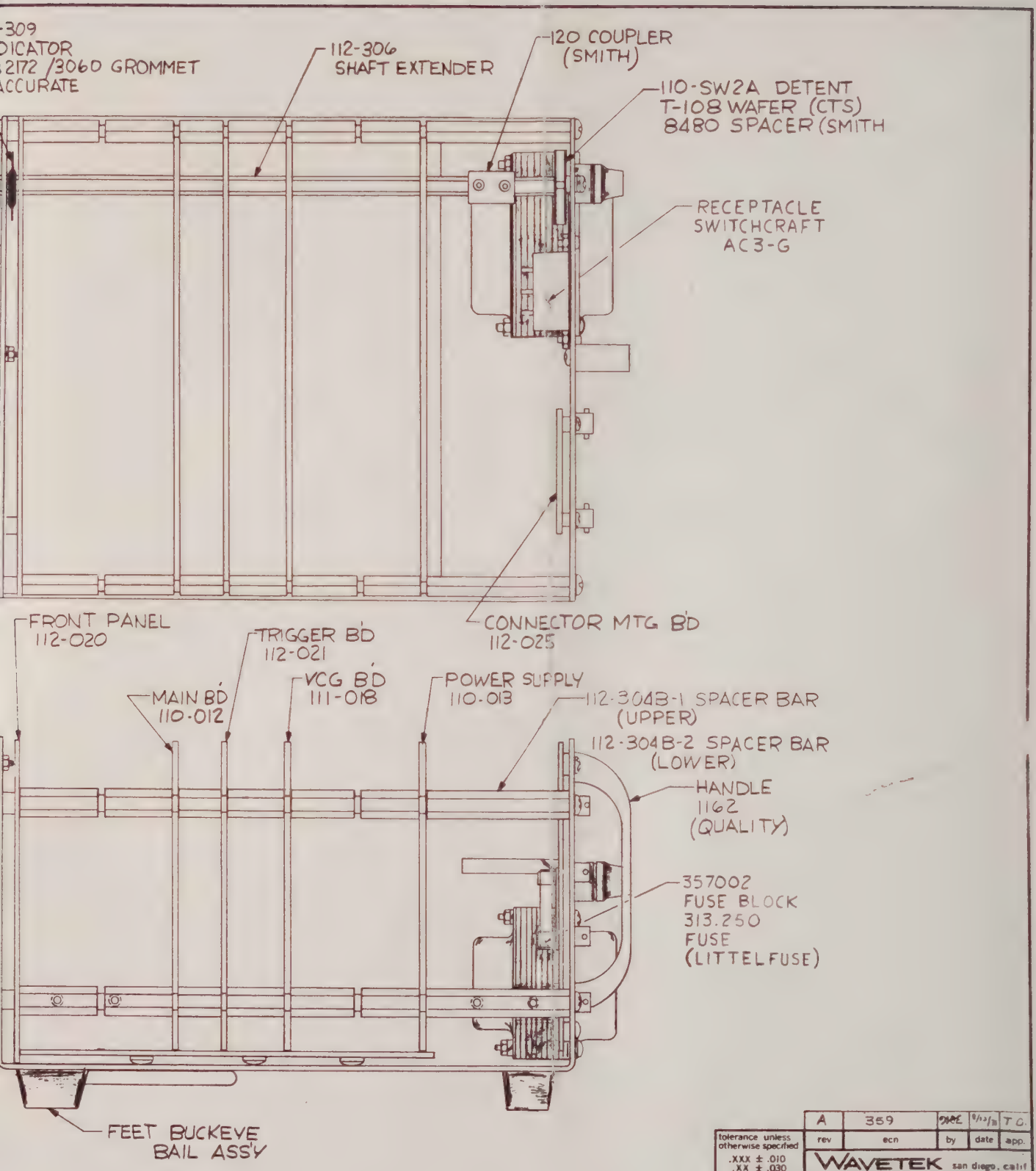
SECTION V
SCHEMATIC DIAGRAMS



115/230 V SWITCH WIRING

115/230 VAC Switch Wiring Schematic Diagram


selected
offset
Zero Adjust
3AG 3/4 AMP
sync
110-310
GUIDE TUBE
5115-25 LOCK RING
(TRUARC)
342012 FUSEHOLDER
312.750 FUSE
(LITTELFUSE)
110-500
TRANSFORMER
112-303
COVER
012-002 DIAL INDICATOR
010-002A DIAL KNOB
130-333 FREQ DIAL
110-312
KNOB
112-301
KNOB
112-302
KNOB
WAVETEK
San diego calif
Triggered VCG
Model 112
off X.3 X1
start/stop point
Freq Hz
X10 X100
X1 X1K
X.1 X10K
X.01 X100K
vernier
cal
-90° +90°
atten
112-300
CHASSIS
slope
gated
cont trig
man
trig
out
VCG in
mode
trig
in
level
Trigger
110-306
BINDING
POST



	A	359		9/13/67	T.C.
tolerance unless otherwise specified .XXX ± .010 .XX ± .030	rev	ecn	by	date	app.
	WAVETEK san diego, calif				
scale 1/1	by M Bachman	date 9-18-67	app		
material	title CHASSIS ASS'Y				
finish	model no. 112	dwg no D112-000	rev A		

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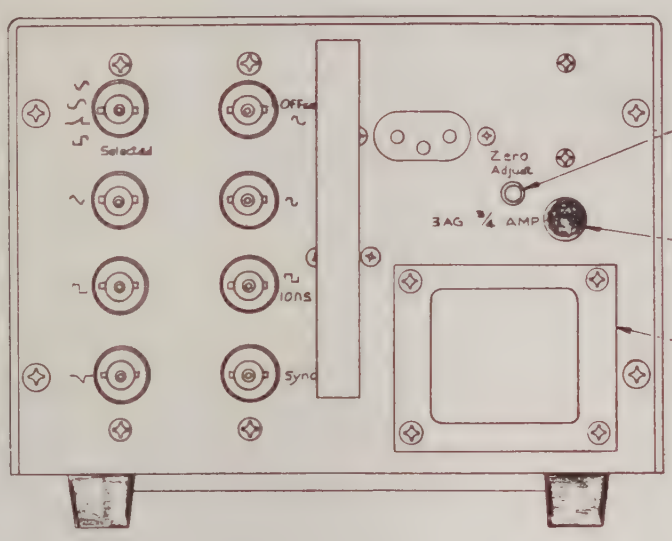


110-310
GUIDE TUBE
5115-25 LOCK RING
(TRUARC)

342012 FUSEHOLDER
312.750 FUSE
(LITTELFUSE)

110500
TRANSFORMER
(COVER SUPPLIED)

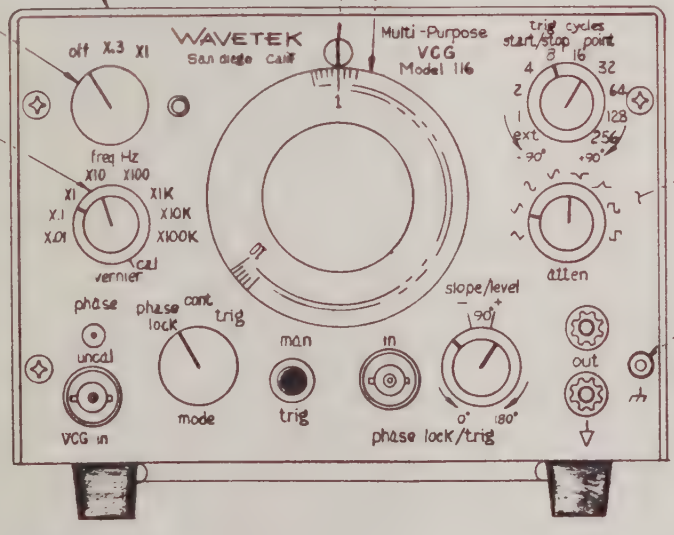
112-303
COVER

012-002
DIAL INDICATOR

010-002 DIAL KNOB
130-333 FREQ-DIAL

110-312
KNOB

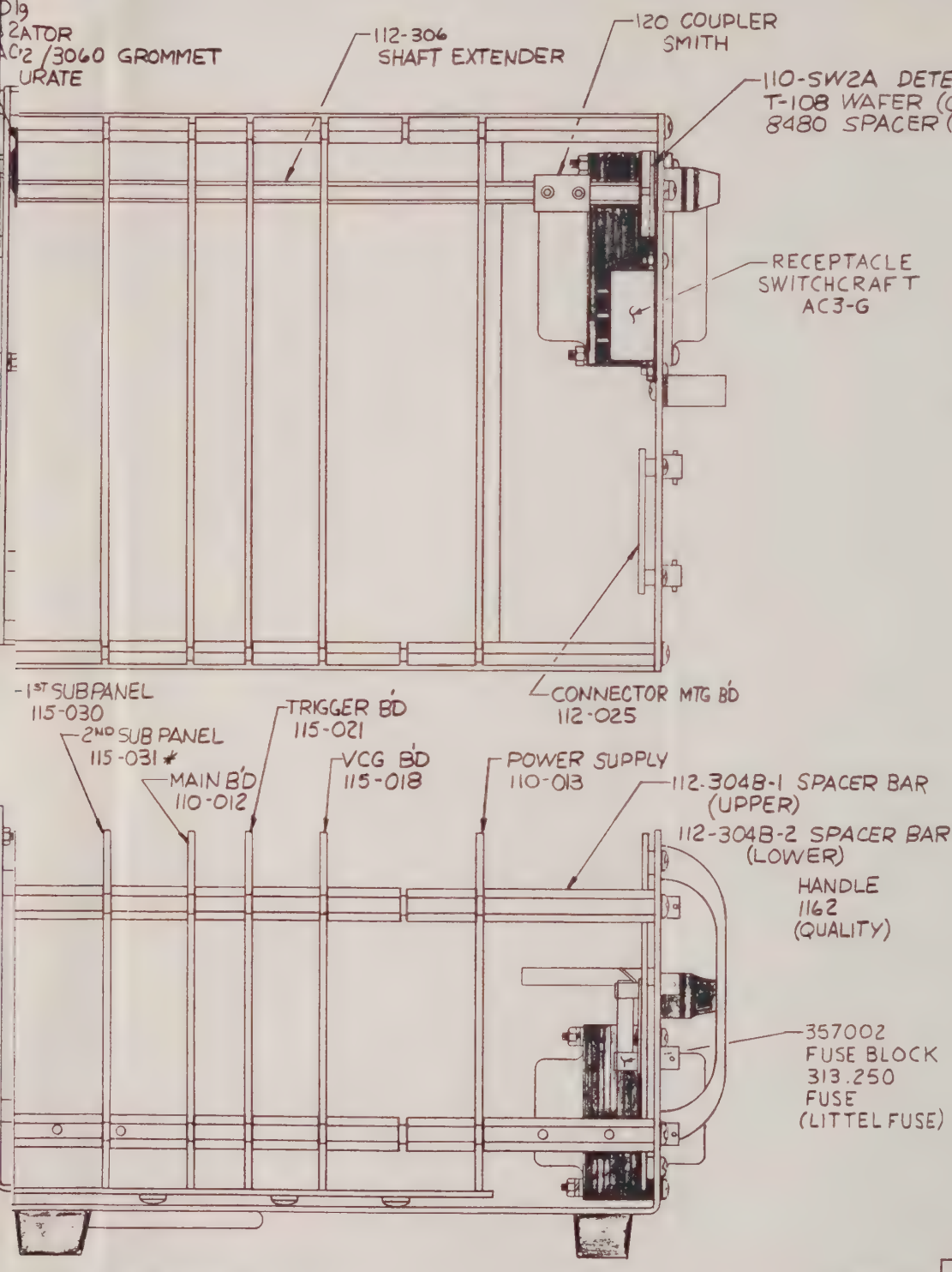
112-301
KNOB
112-302
KNOB



115-300
CHASSIS

110-306
BINDING
POST

* FOR 116 MODEL USE ASSEMBLY 116-031



	A	359		6/10/71	T.O.
tolerance unless otherwise specified .XXX ± 010 .XX ± 030	rev	ecn	by	date	app.
	WAVETEK san diego, calif				
scale 1:1	by ME Br	date 6-28-67	app		
material	title CHASSIS ASSY				
finish	model no. 115,116	dwg no. 0115-000		rev A	

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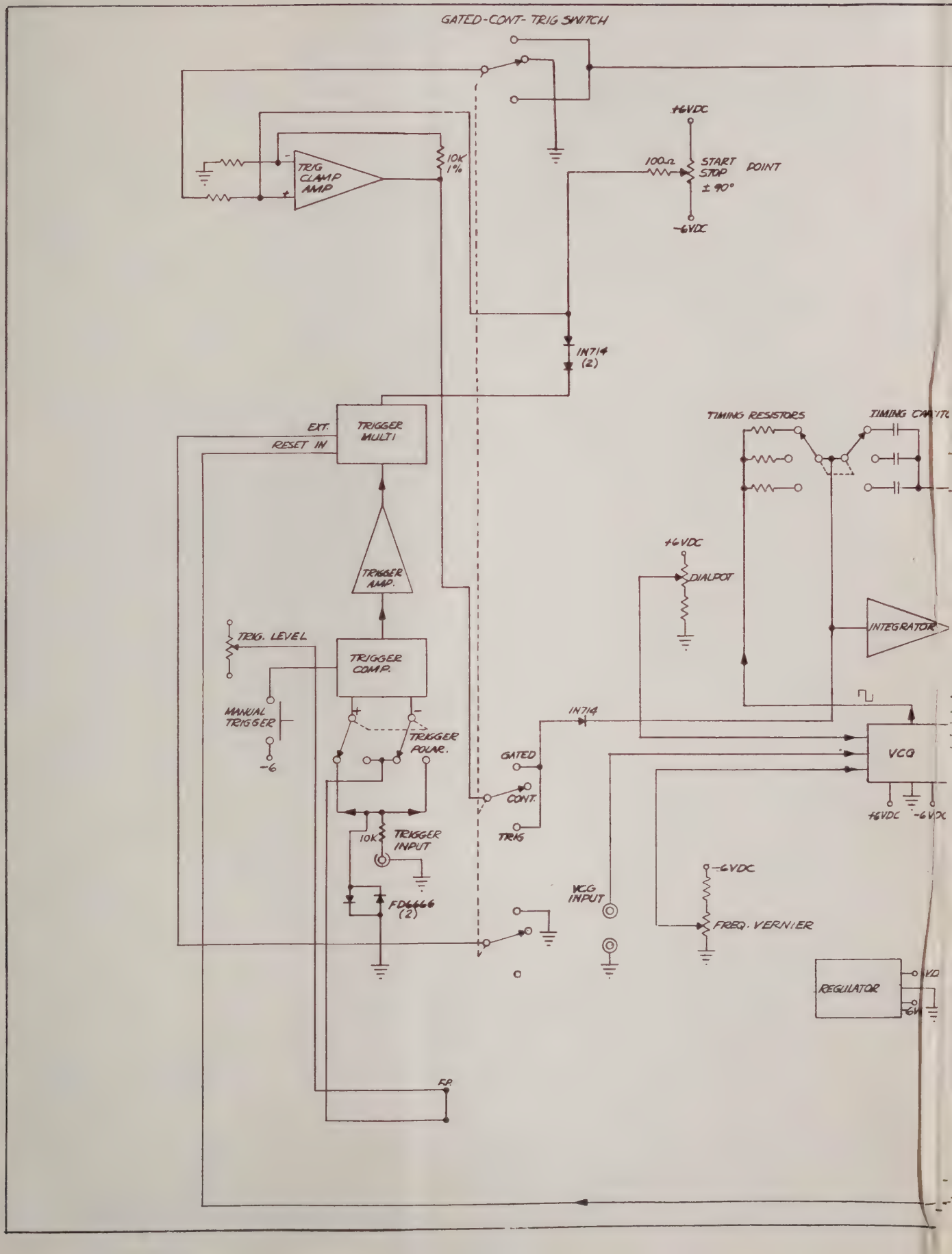
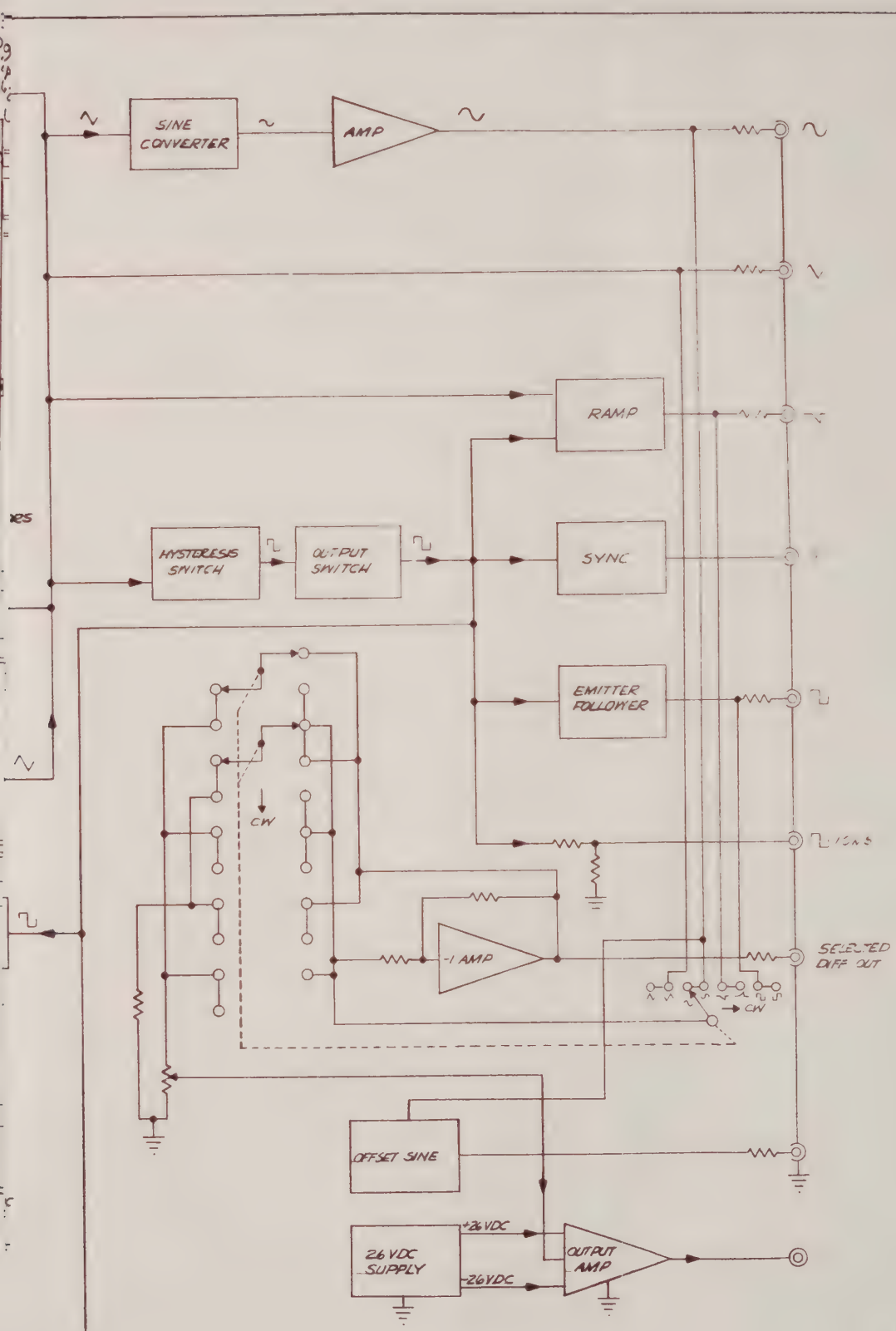

GATED-CONT-TRIG SWITCH
+6VDC
100Ω
START STOP POINT
± 90°
-6VDC
TRIG CLAMP AMP
10K 1%
IN714 (2)
EXT.
RESET IN
TRIGGER MULTI
TRIGGER AMP.
TRIG. LEVEL
TRIGGER COMP.
MANUAL TRIGGER
-6
TRIGGER POLAR.
GATED
CONT.
TRIG
10K
TRIGGER INPUT
FD6466 (2)
IN714
TIMING RESISTORS
TIMING CAPACITOR
+6VDC
DIALPOT
INTEGRATOR
VCG
+6VDC
-6VDC
VCG INPUT
-6VDC
FREQ. VERNIER
REGULATOR
+VO
-6V
F.F.

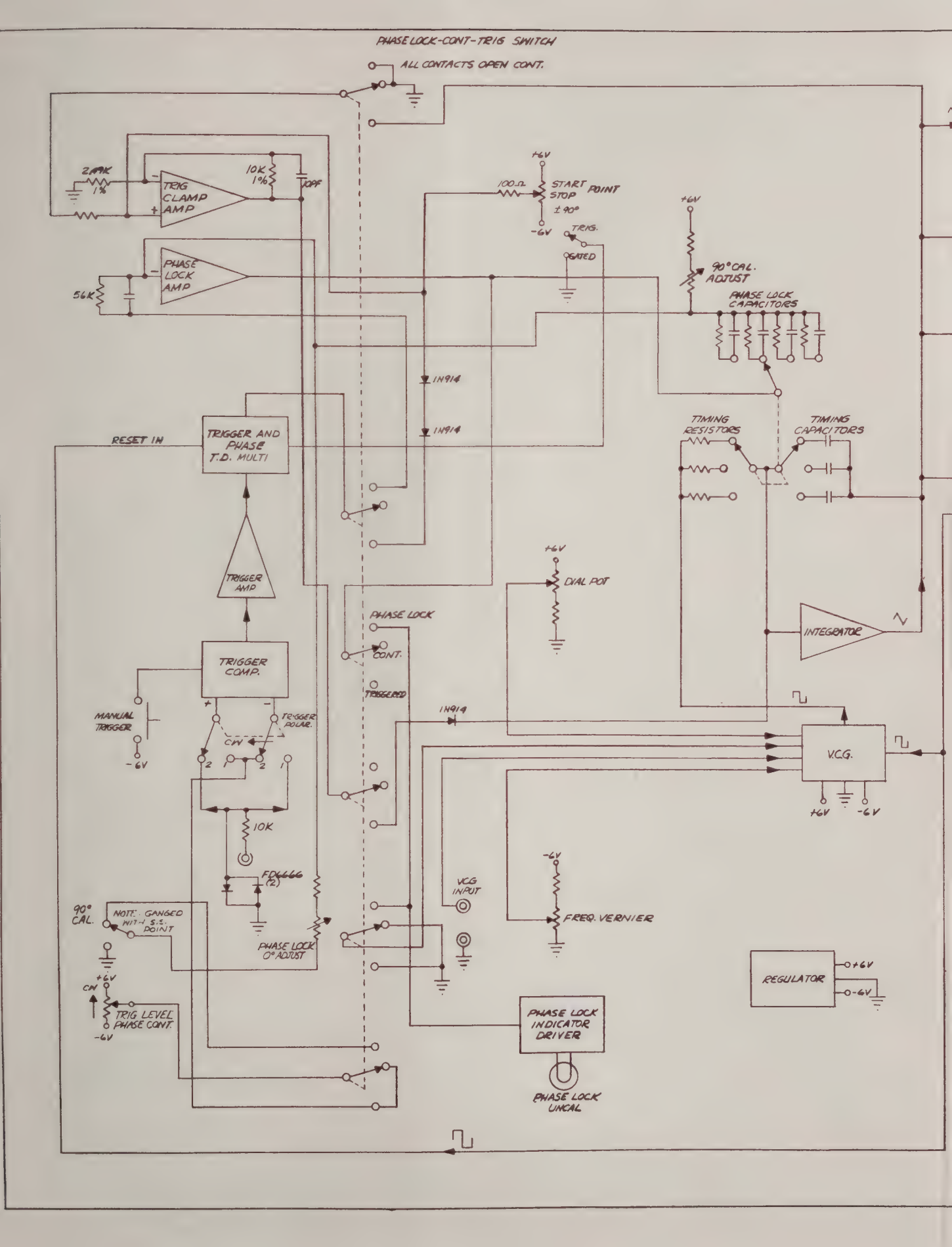


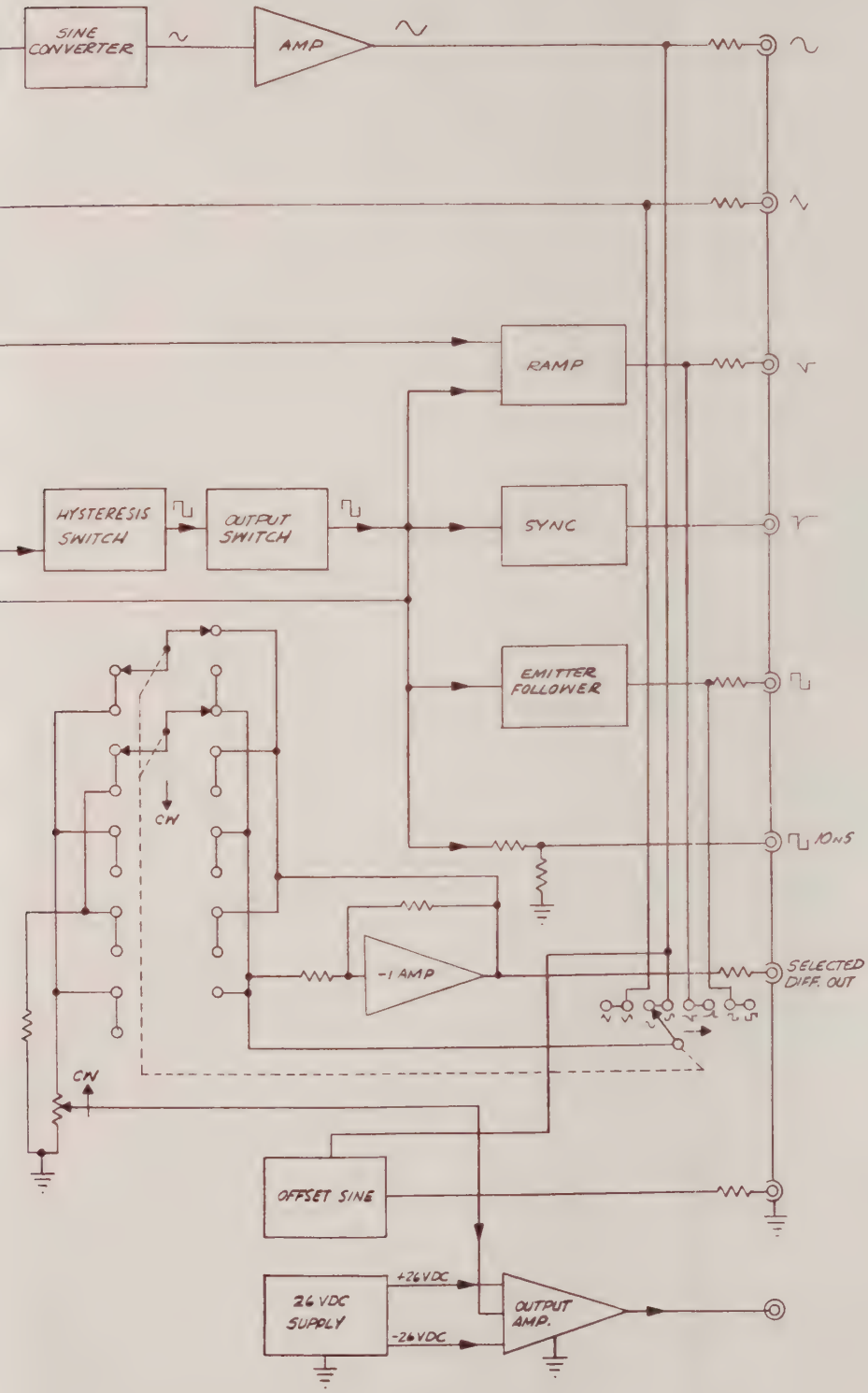
WAVETEK 8159 engineering sandiego, calif.

dwn: MATTOCK date 5-9-66 appd: P Mackie

BLOCK DIAGRAM TRIGGERED VCG

model: 112 no: 112-600

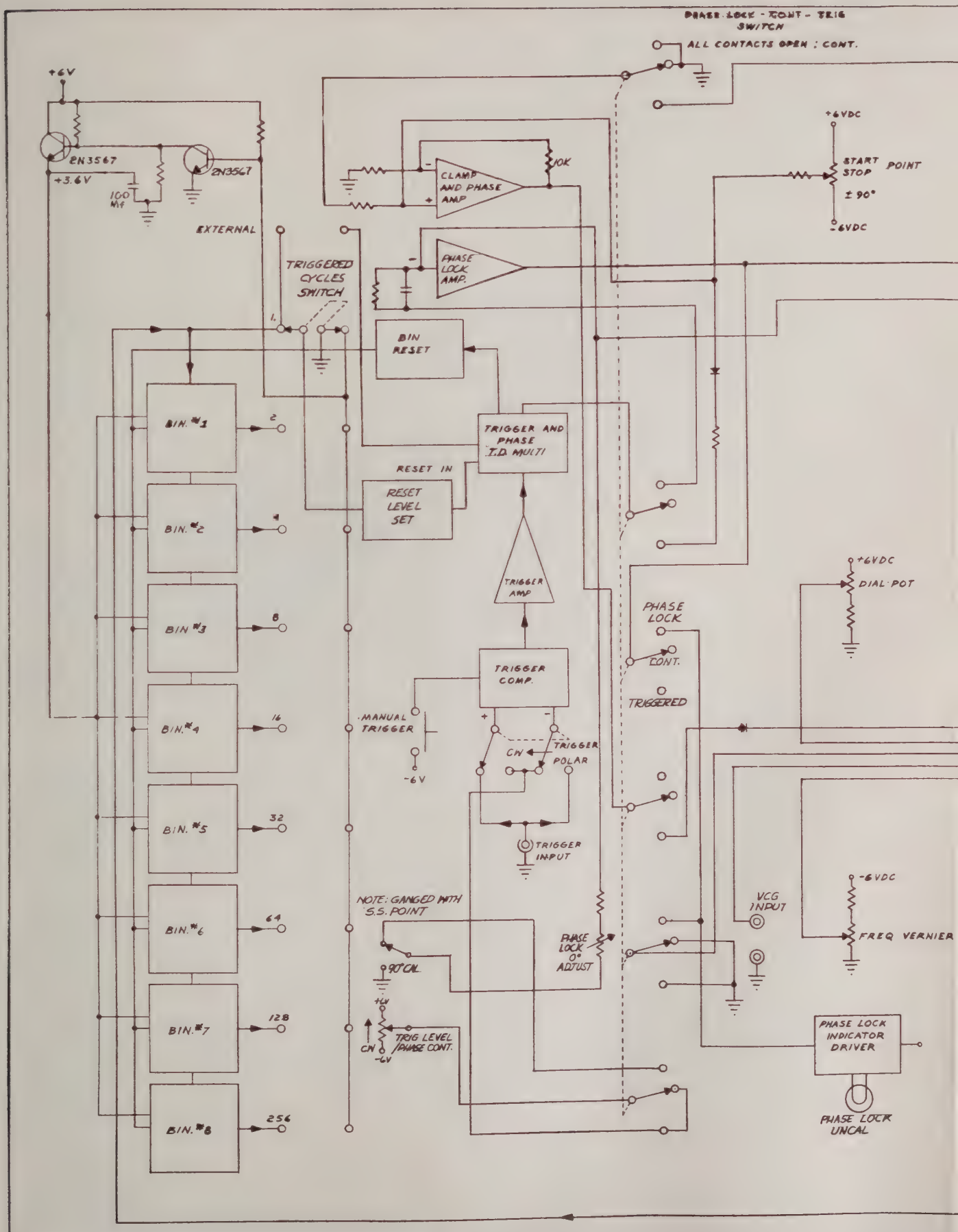

PHASE LOCK-CONT-TRIG SWITCH
ALL CONTACTS OPEN CONT.
2.49K 1%
10K 1%
.001
TRIG CLAMP AMP
PHASE LOCK AMP
56K
+6V
100Ω
START STOP POINT
±90°
-6V
TRIG.
GATED
90° CAL. ADJUST
PHASE LOCK CAPACITORS
1N914
1N914
RESET IN
TRIGGER AND PHASE T.D. MULTI
TIMING RESISTORS
TIMING CAPACITORS
TRIGGER AMP
+6V
DIAL POT
PHASE LOCK
CONT.
TRIGGERED
INTEGRATOR
TRIGGER COMP.
MANUAL TRIGGER
-6V
TRIGGER POLAR.
CW
1N914
V.C.G.
+6V
-6V
10K
FDH666 (2)
VCG INPUT
-6V
FREQ. VERNIER
90° CAL.
NOTE: GANGED WITH S.S. POINT
PHASE LOCK 0° ADJUST
+6V
CW
TRIG LEVEL PHASE CONT.
-6V
REGULATOR
+6V
-6V
PHASE LOCK INDICATOR DRIVER
PHASE LOCK UNCAL

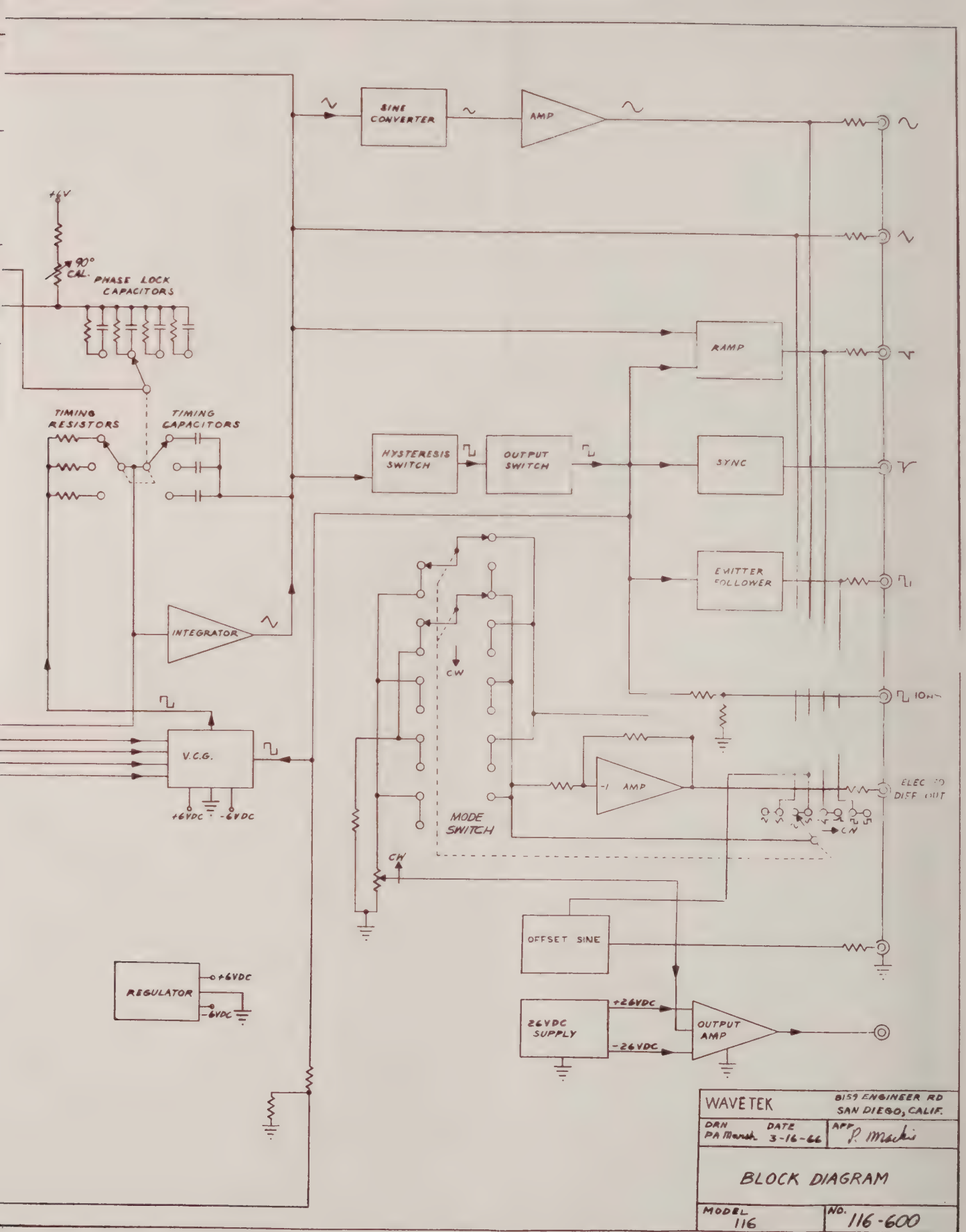


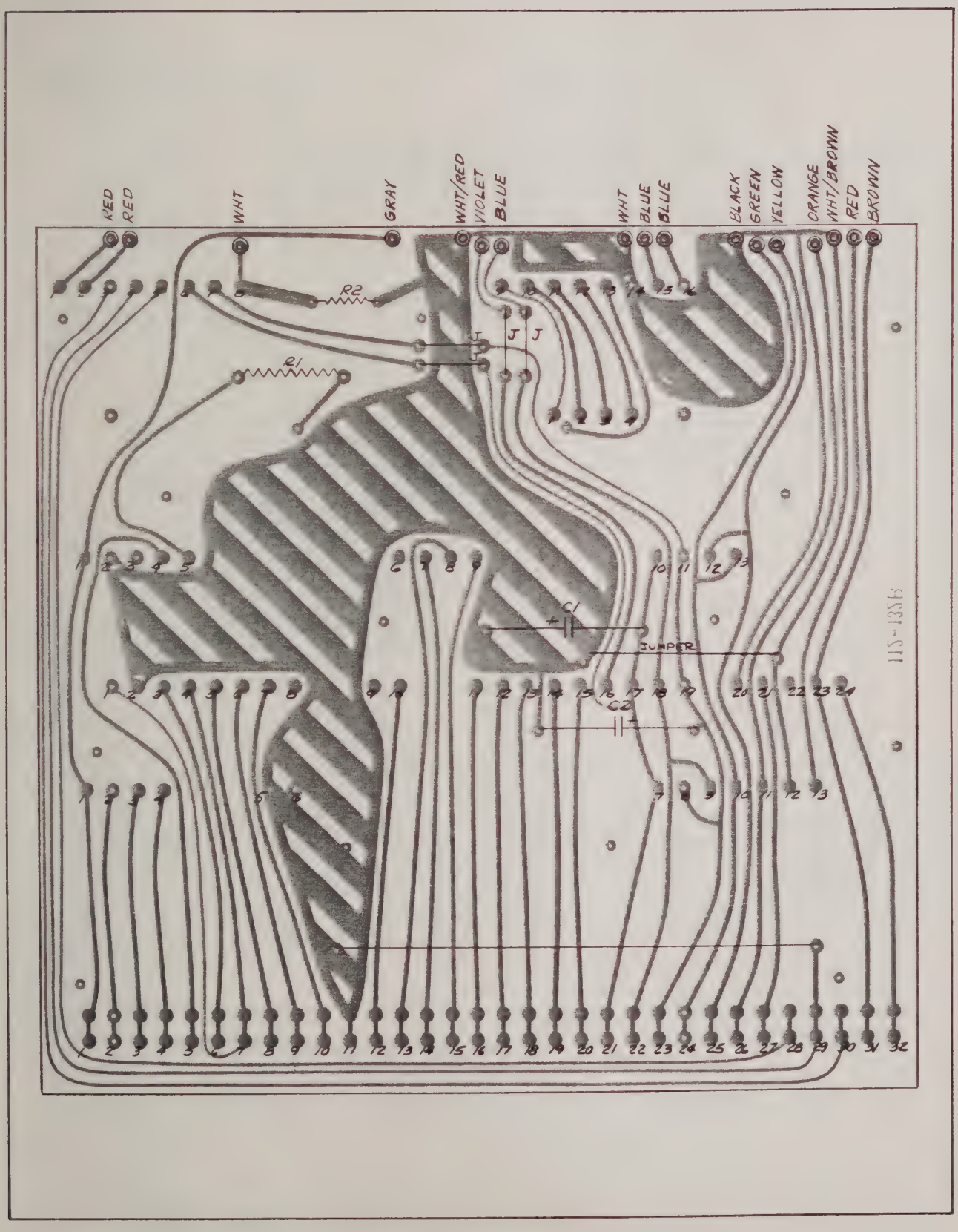
WAVETEK		9559 ENGINEER RD. SAN DIEGO, CALIF
DWN: WHITELOCK	DATE: 6-9-6	APP'D: P. Marks

BLOCK DIAGRAM PHASE LOCK/TRIGGER

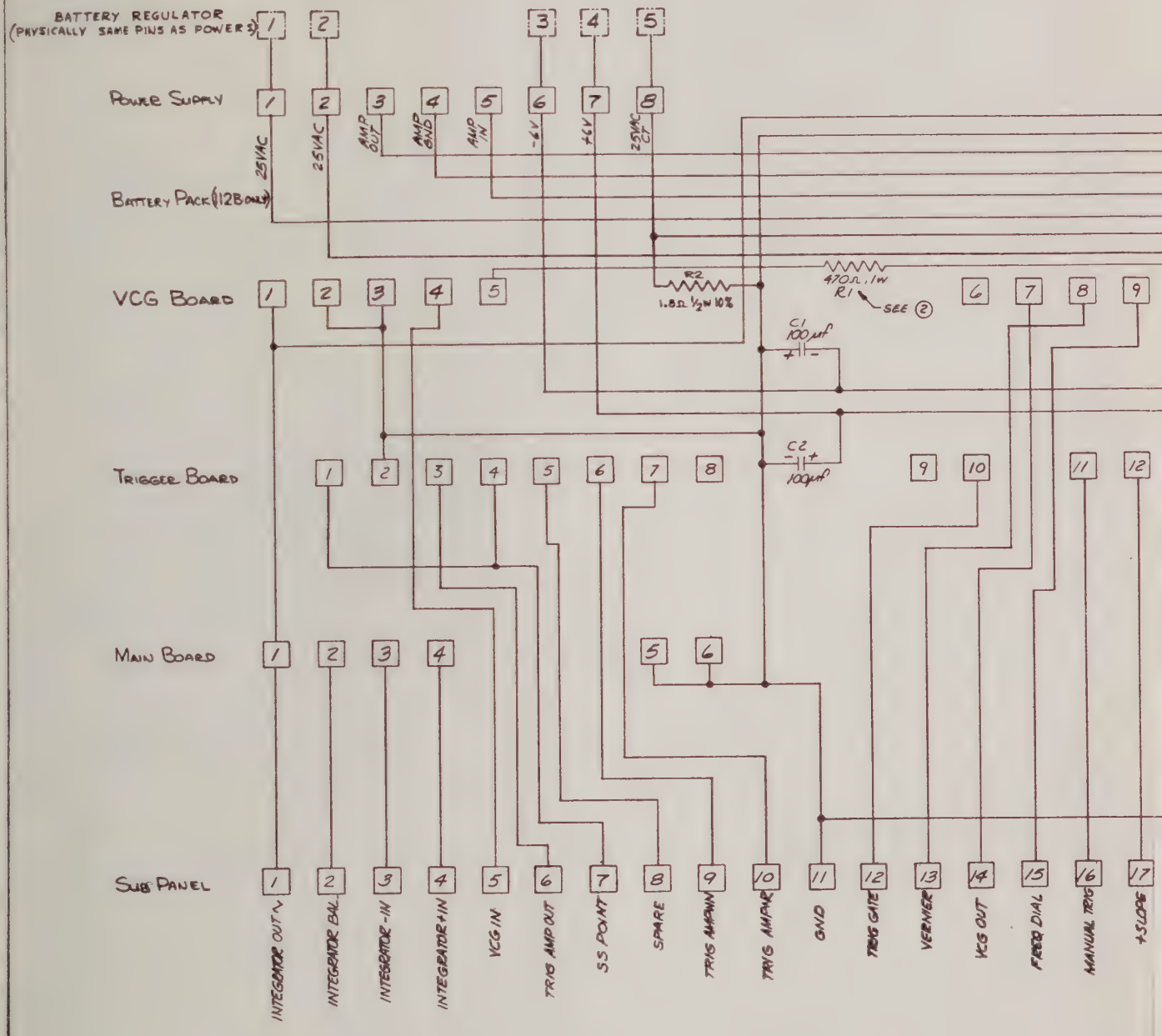
MODEL: 115	NO: 115-600


PHASE LOCK - CONT - TRIG SWITCH
ALL CONTACTS OPEN : CONT.
+6V
2N3567
2N3567
+3.6V
100 Mf
EXTERNAL
CLAMP AND PHASE AMP
10K
+6VDC
START STOP POINT
± 90°
-6VDC
PHASE LOCK AMP.
TRIGGERED CYCLES SWITCH
BIN RESET
BIN #1
BIN #2
BIN #3
BIN #4
BIN #5
BIN #6
BIN #7
BIN #8
2
4
8
16
32
64
128
256
TRIGGER AND PHASE I.D. MULTI
RESET IN
RESET LEVEL SET
TRIGGER AMP.
TRIGGER COMP.
MANUAL TRIGGER
-6V
CN
TRIGGER POLAR
TRIGGER INPUT
+6VDC
DIAL POT
PHASE LOCK
CONT.
TRIGGERED
NOTE: GANGED WITH S.S. POINT
90° CAL.
+6V
CN
-6V
TRIG LEVEL / PHASE CONT.
PHASE LOCK 0° ADJUST
VCG INPUT
-6VDC
FREQ VERNIER
PHASE LOCK INDICATOR DRIVER
PHASE LOCK UNCAL


SINE CONVERTER
AMP
+6V
90° CAL.
PHASE LOCK CAPACITORS
TIMING RESISTORS
TIMING CAPACITORS
RAMP
HYSTERESIS SWITCH
OUTPUT SWITCH
SYNC
EMITTER FOLLOWER
INTEGRATOR
CW
10H
V.C.G.
+6VDC
-6VDC
-1 AMP
ELEC TO DIFF OUT
CW
MODE SWITCH
CW
OFFSET SINE
REGULATOR
+6VDC
-6VDC
26VDC SUPPLY
+26VDC
-26VDC
OUTPUT AMP
WAVETEK
8159 ENGINEER RD
SAN DIEGO, CALIF.
DRN PA Marsh
DATE 3-16-66
APP'D P. Machi
BLOCK DIAGRAM
MODEL 116
NO. 116-600



Model 112 Mother Board Assembly (112-032)

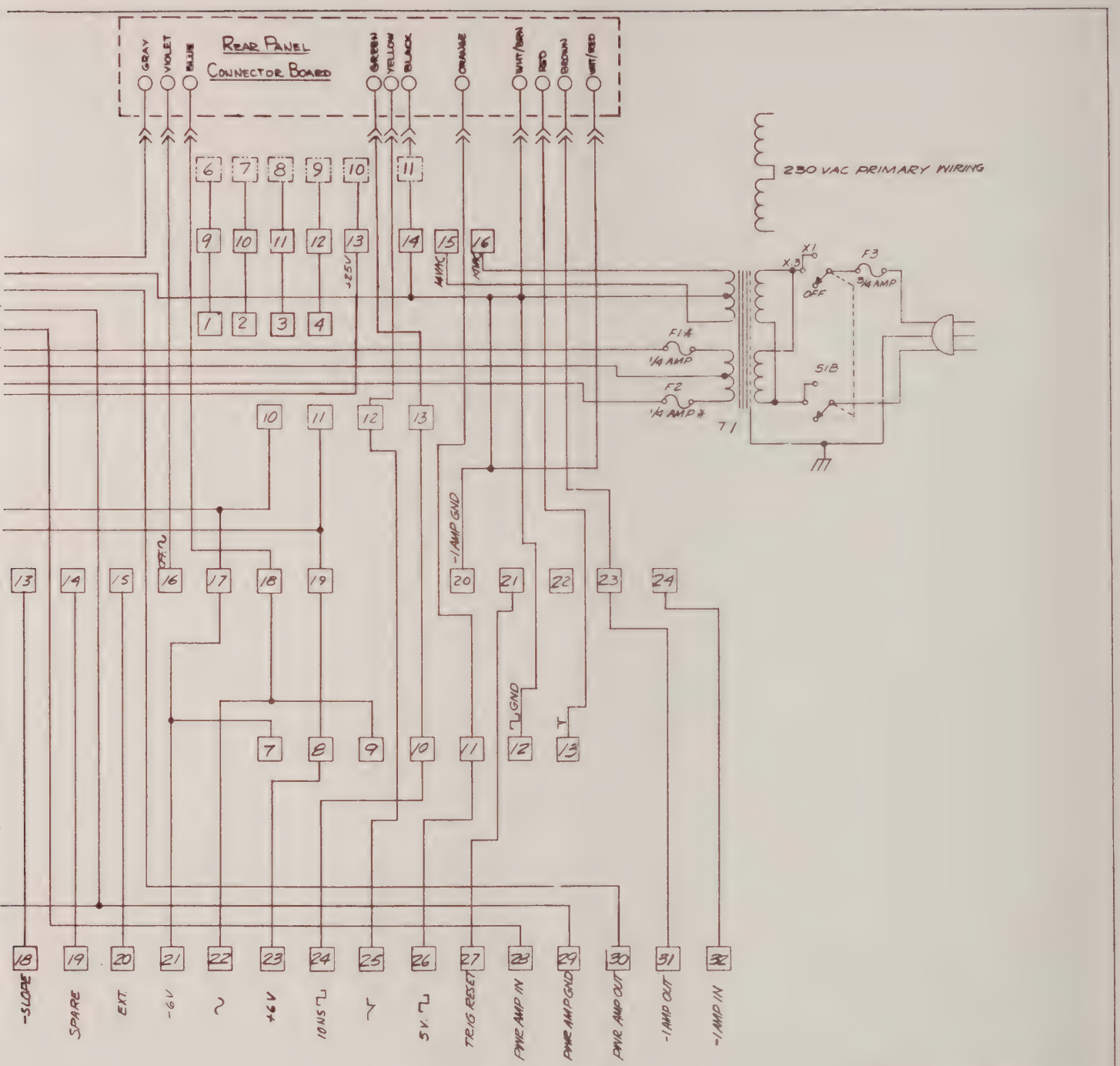


NOTE:

1 PINS ARE NUMBERED LEFT TO RIGHT AS VIEWED FROM COMPONENT SIDE OF BOARD.

(2) FOR "B" MODELS REPLACE R1 WITH A JUMPER

3(#) F1 & F2 ARE 1 AMP S.B. FOR (112, 114/115 & 116) B.



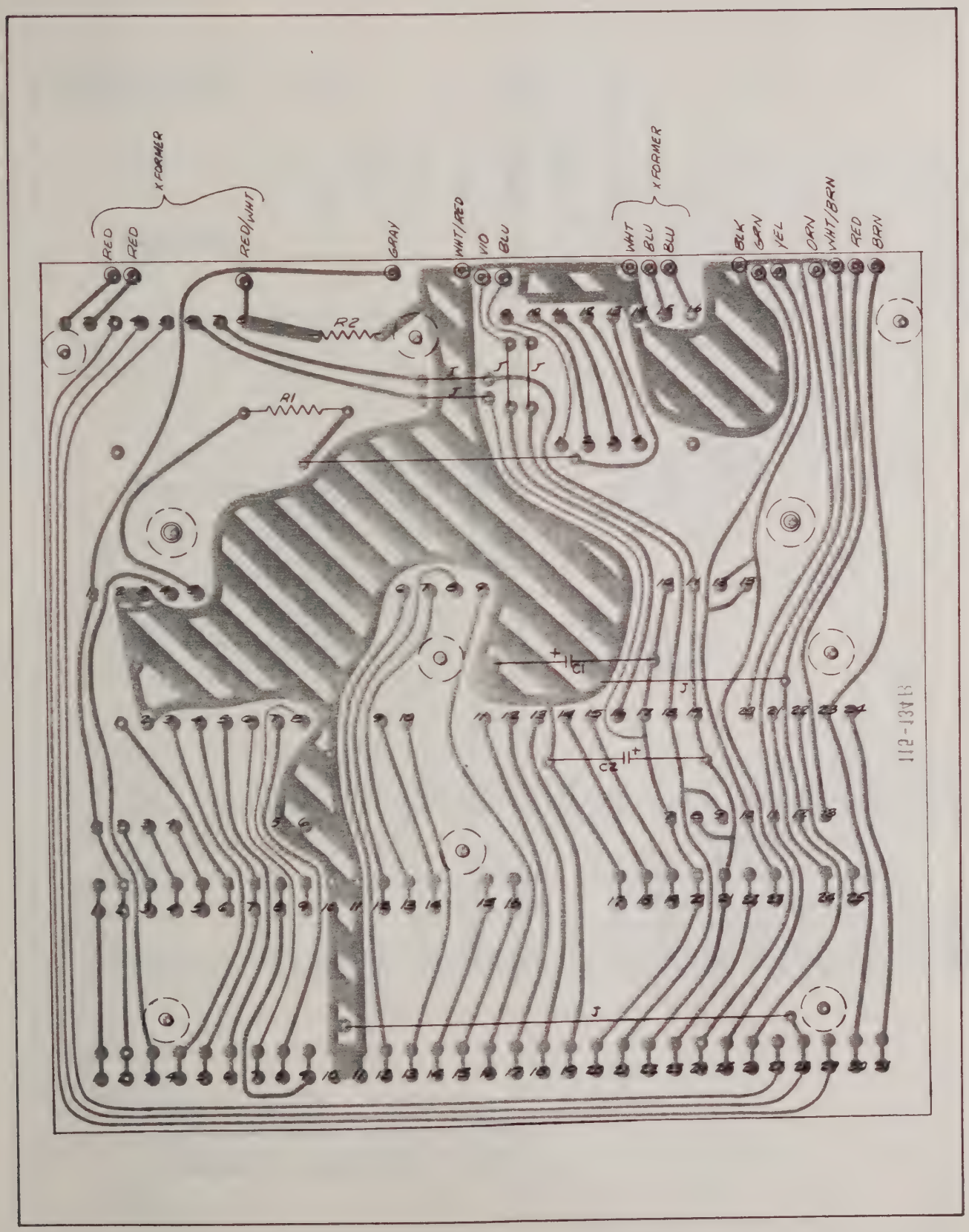
CHG	ECN NO	BY	DATE	APP
G	ECN 291	[illegible]	1-6-70	T.O
F	ECN #166	[illegible]	9/7/67	T O
E	ECN #167	ENH	9-5-67	T O
D	ECN #162	[illegible]	7-26-67	T.O.
C	ECN #146	MSB	6-21-67	T O
B	128	PM	3-16-67	T.O.
A	112 (WAS DWG 112-219)	JW	1-5-67	T O.

WAVETEK SAN DIEGO, CALIF.

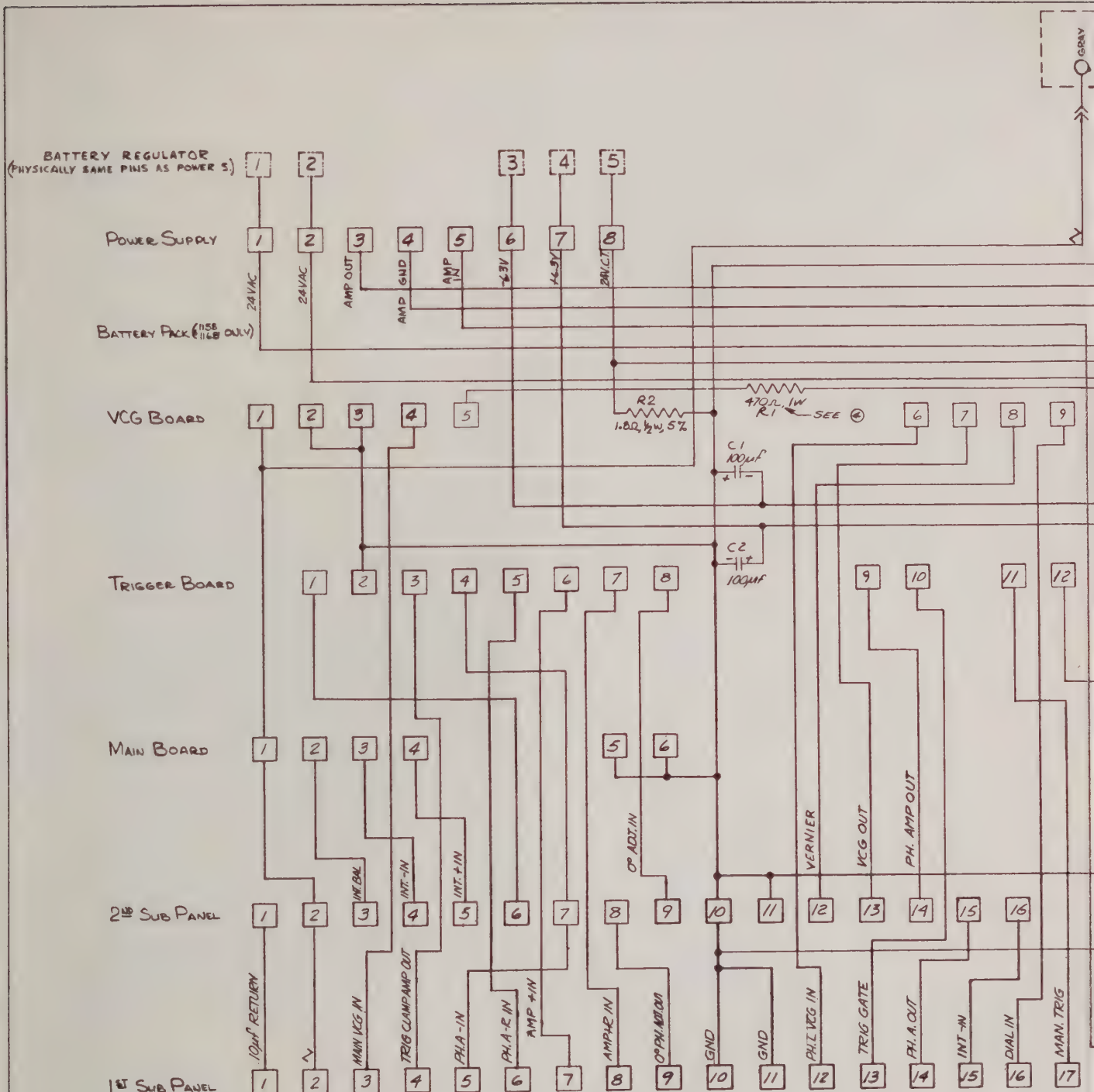
DWN: WHITELOCK DATE: 5-25-6 APP'D: [illegible]

MOTHER BOARD

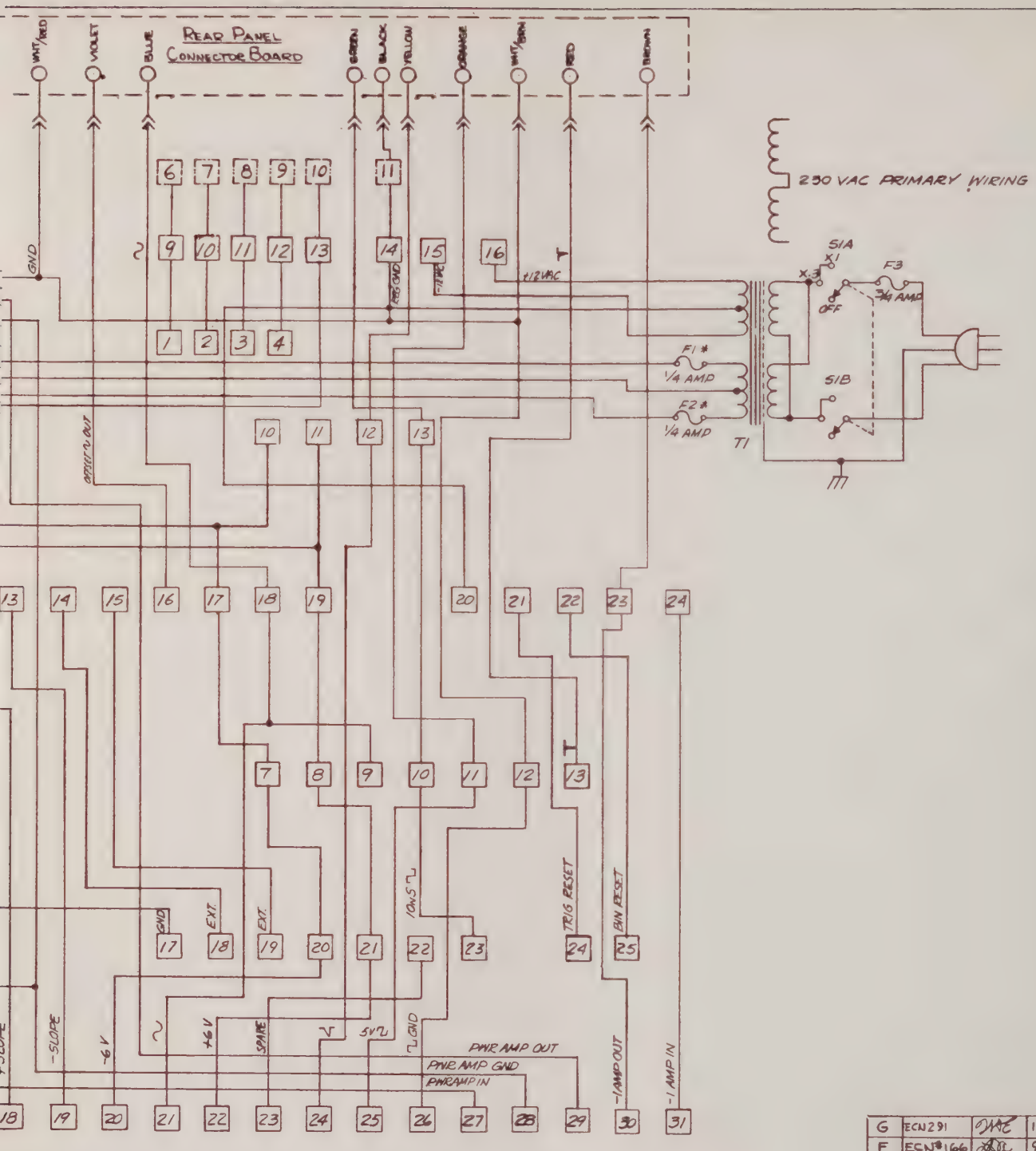
MODEL: 112 NO: 01/12-232G



Model 115 & 116. Mother Board Assembly (115-034)



NOTE:
1. PINS ARE NUMBERED FROM LEFT TO RIGHT AS VIEWED FROM COMPONENT SIDE OF BOARD.
2. (*) F1 & F2 ARE 1 AMP Q.B. FOR (112, 114, 115 & 116)B.
3. ⊕ FOR 115B-116B* MODELS REPLACE R1 WITH A JUMPER



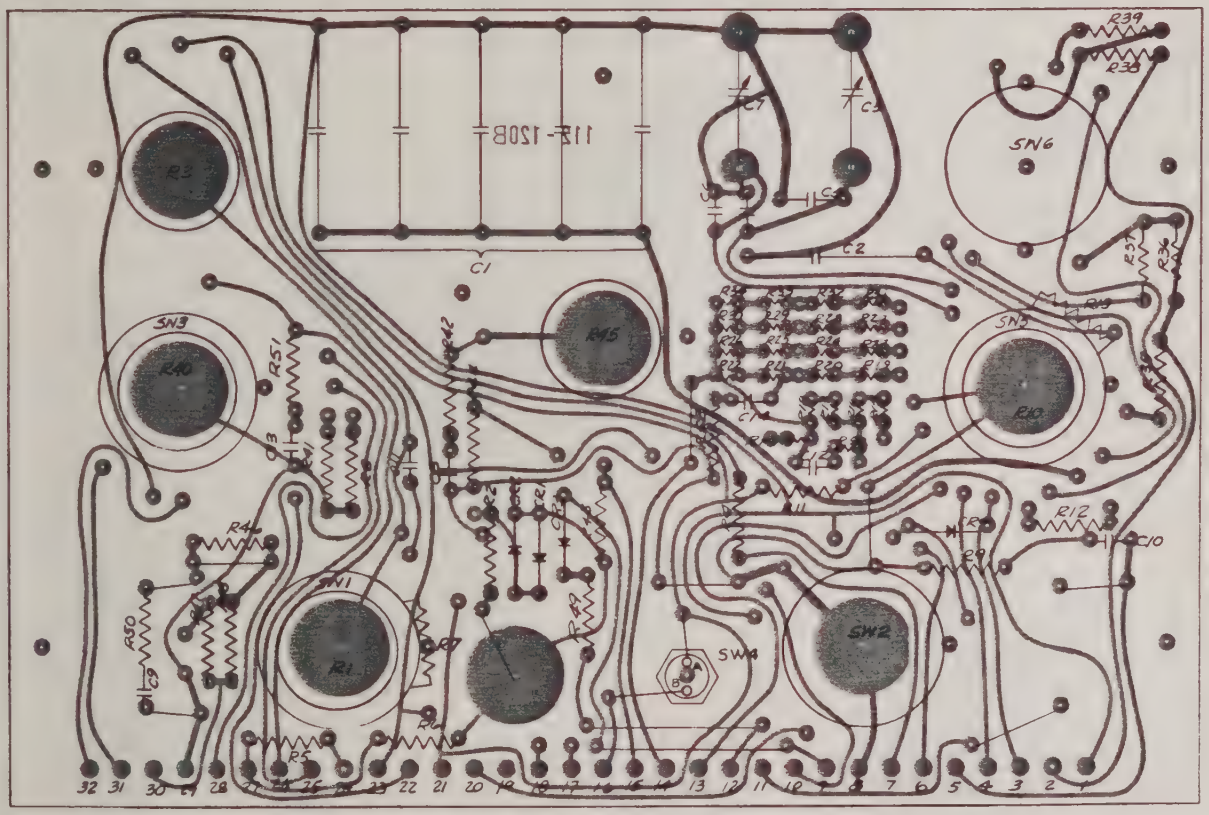
CHG	ECN NO.	BY	DATE	APP'D
G	ECN 291	DAE	1-6-70	T.O
F	ECN #166	DAE	9/7/67	T.O.
E	ECN #167	ENH	9-5-67	T.O.
D	ECN #162	DAE	7-26-67	T.O.
C	146	MEB	6-22-67	T.O.
B	128	PAM	3-16-67	T.O.
A	112 (and 115-229)	JW	1-5-67	T.O.

WAVETEK SAN DIEGO, CALIF.

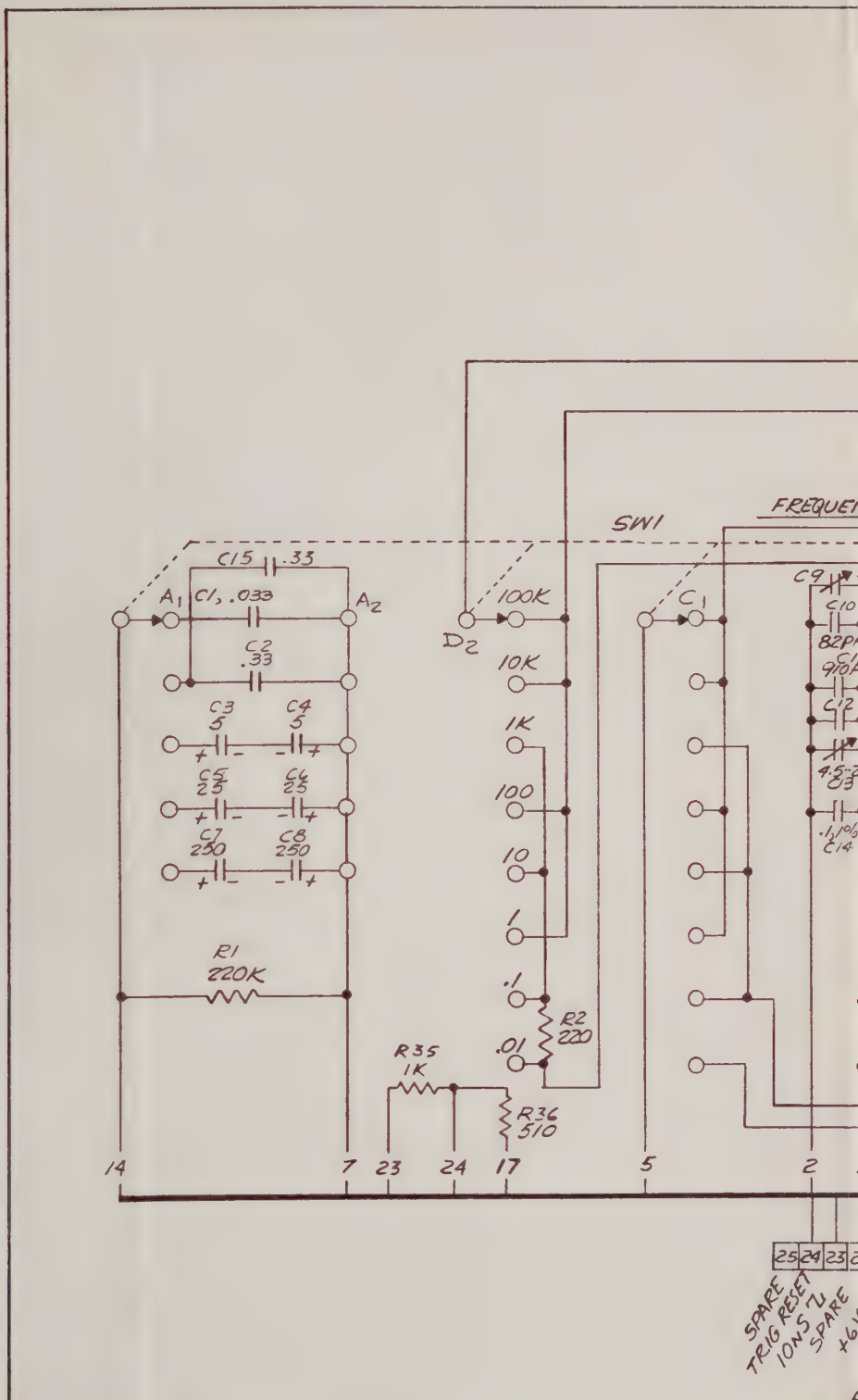
DWN: WHITELOCK DATE: 5-24-6 APP'D: J. Mackie

MOTHER BOARD

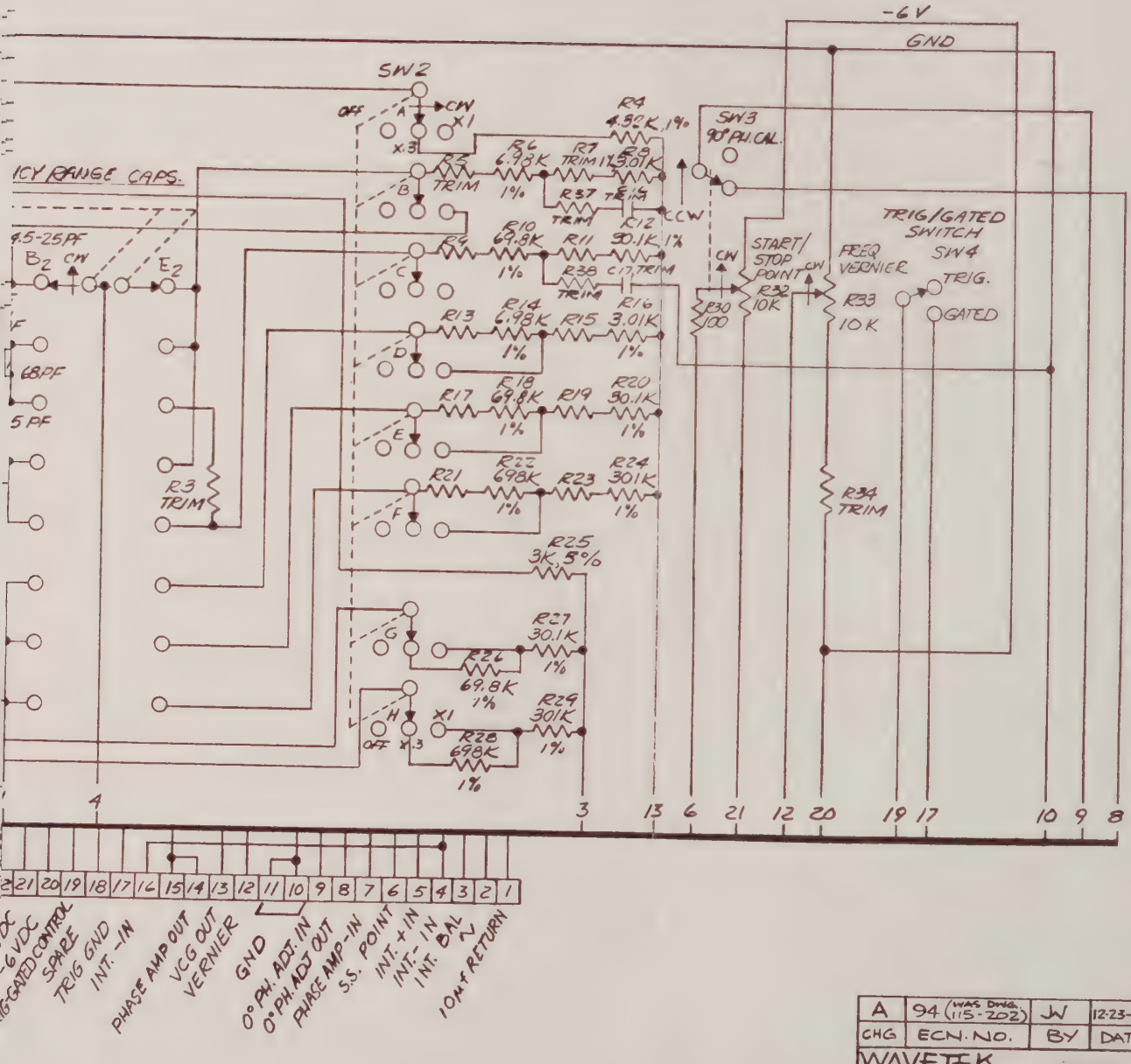
MODEL: 115 & 116 NO. D115-2346



Model 112. Front Panel Assembly (112-020)



NOTE: UNLESS OTHERWISE SPECIFIED
1. RESISTANCE IN OHMS, 1/2W, 10%.
2. CAPACITANCE IN MICROFARADS
3. PINS NUMBERED RIGHT TO LEFT AS VIEWED FROM COMPONENT SIDE OF BOARD



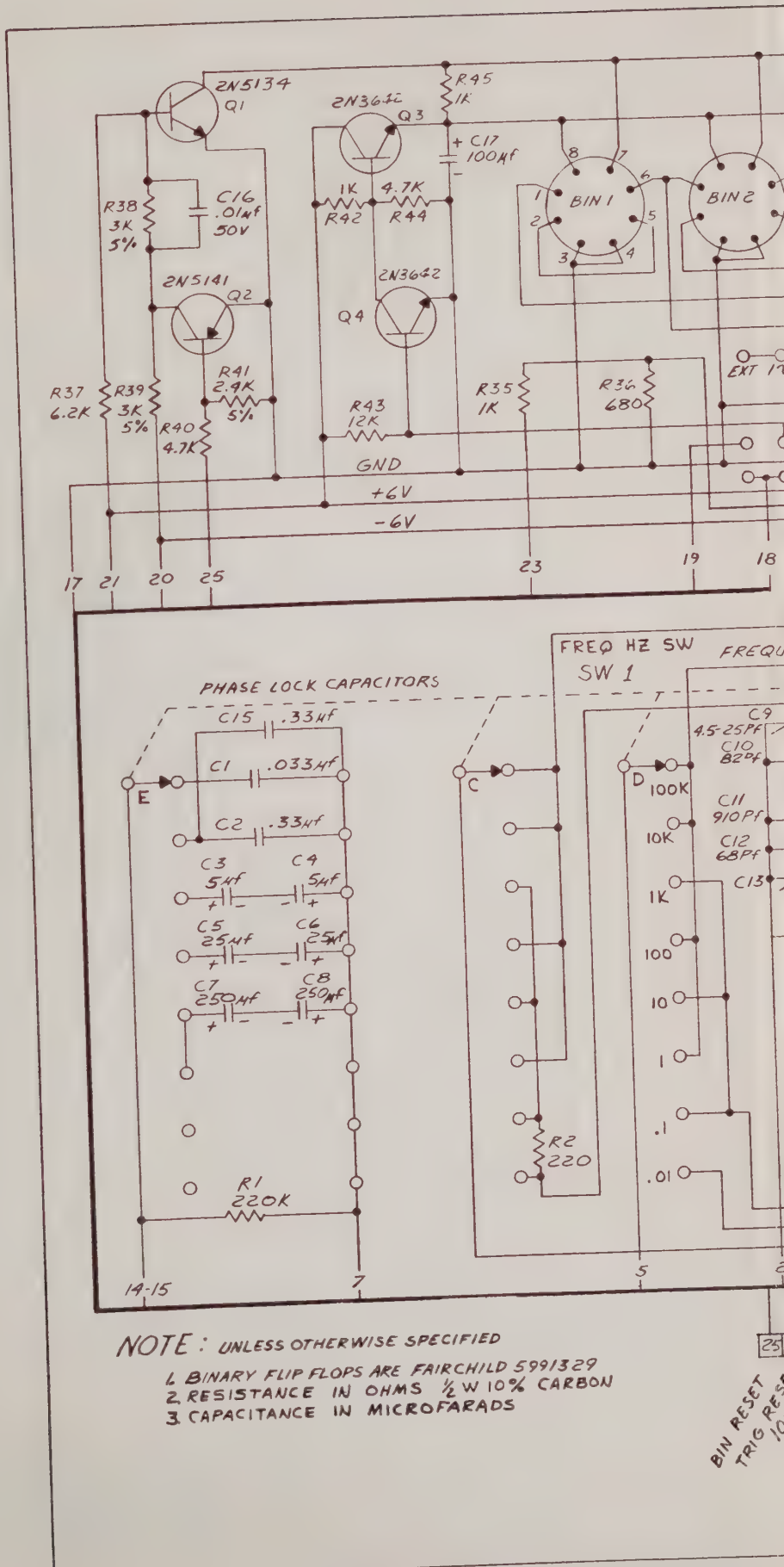
A	94 (WAS DWG. 115-202)	JW	12-23-66	
CHG	ECN. NO.	BY	DATE	APP'D

WAVETEK SAN DIEGO, CALIF

DWN: WHITELOCK DATE: 5-23-6 APP'D: P. Mucki

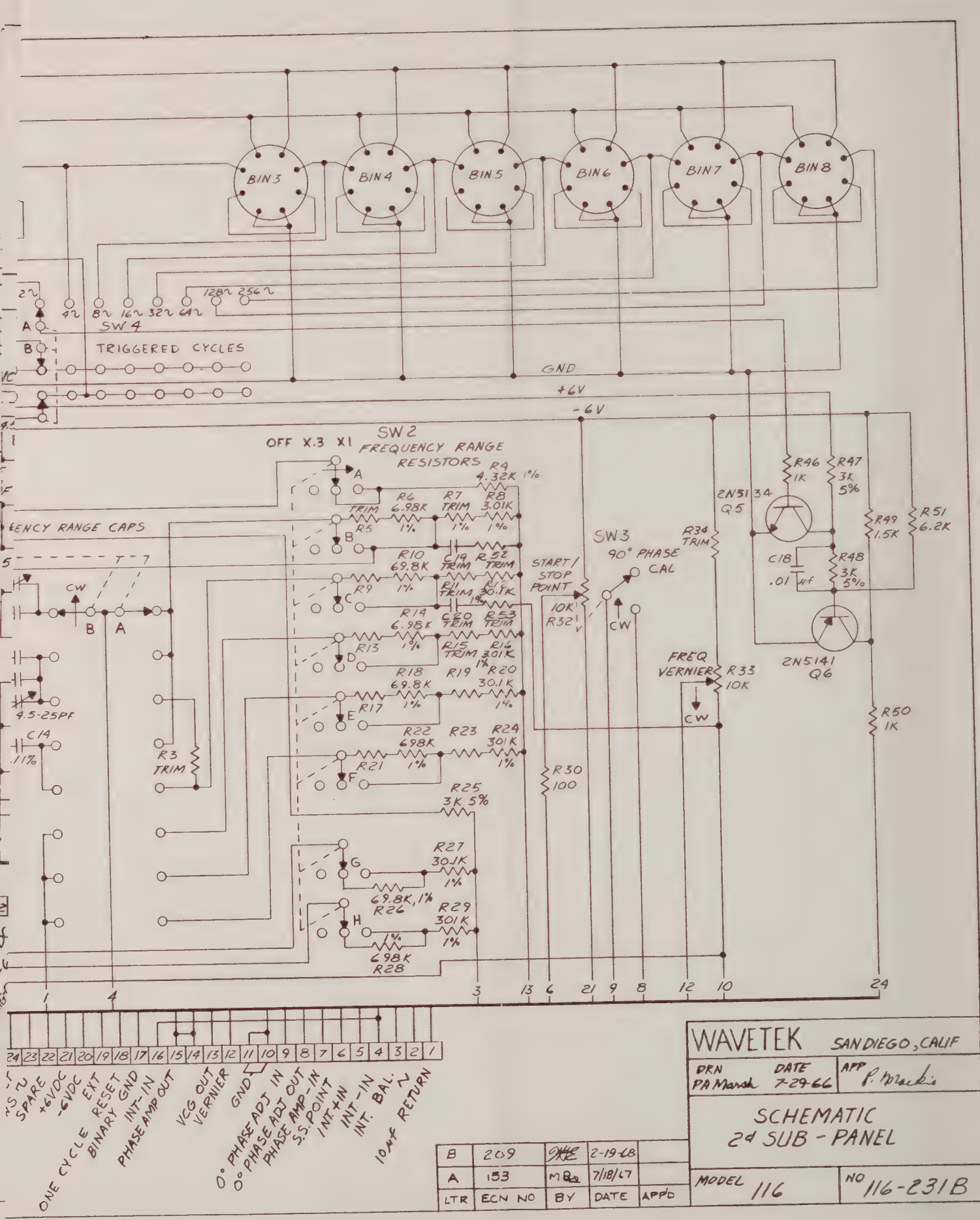
SCHEMATIC - 2ND SUB PANEL

MODEL: 115 NO.: 115-231A



NOTE : UNLESS OTHERWISE SPECIFIED

1. BINARY FLIP FLOPS ARE FAIRCHILD 5991329
2. RESISTANCE IN OHMS ½ W 10% CARBON
3. CAPACITANCE IN MICROFARADS



LTR	ECN NO	BY	DATE	APP'D
B	209	[illegible]	2-19-68	
A	153	MB	7/18/67	

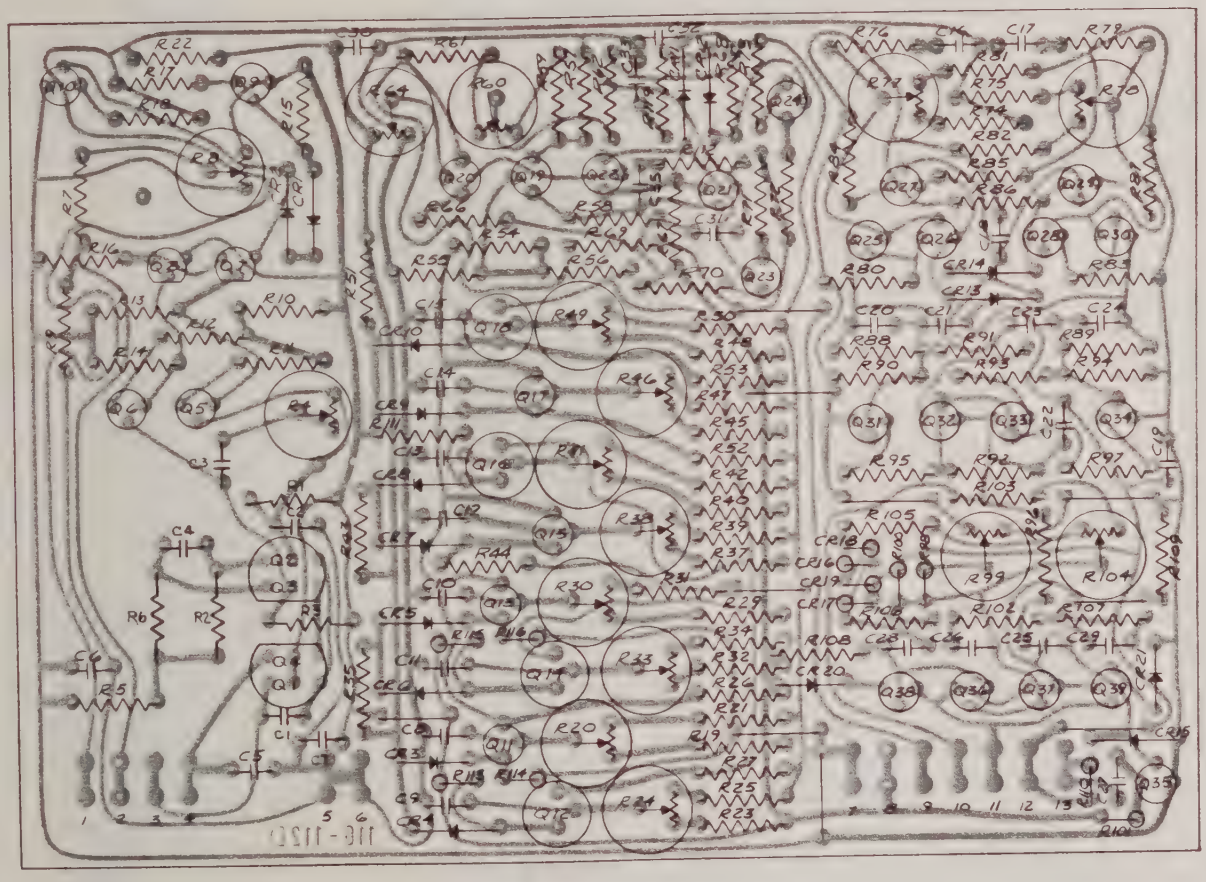
WAVETEK SAN DIEGO, CALIF

DRN	DATE	APP
PA Marsh	7-29-66	P. Mackie

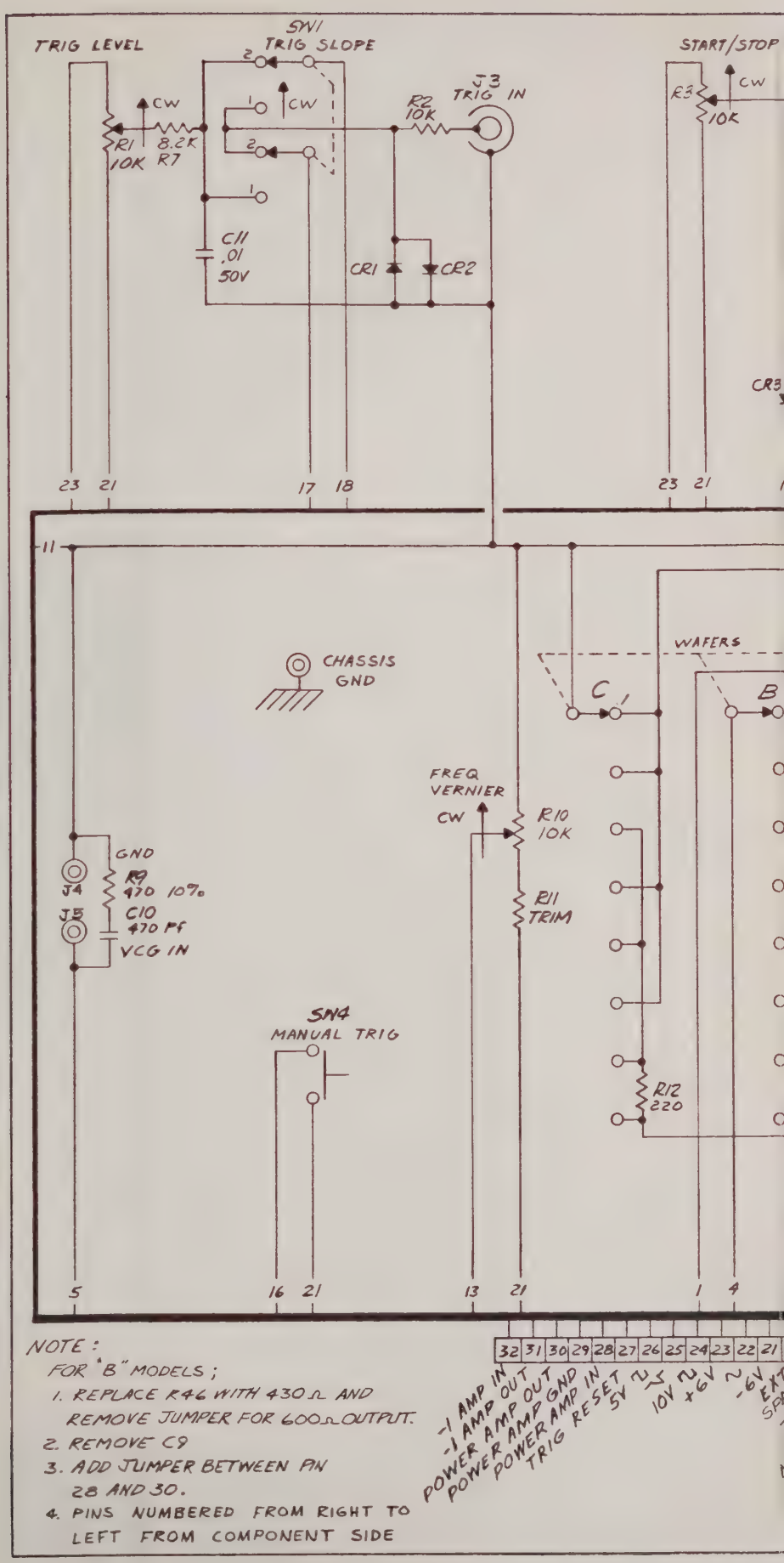
SCHEMATIC
2d SUB - PANEL

MODEL 116

NO 116-231B



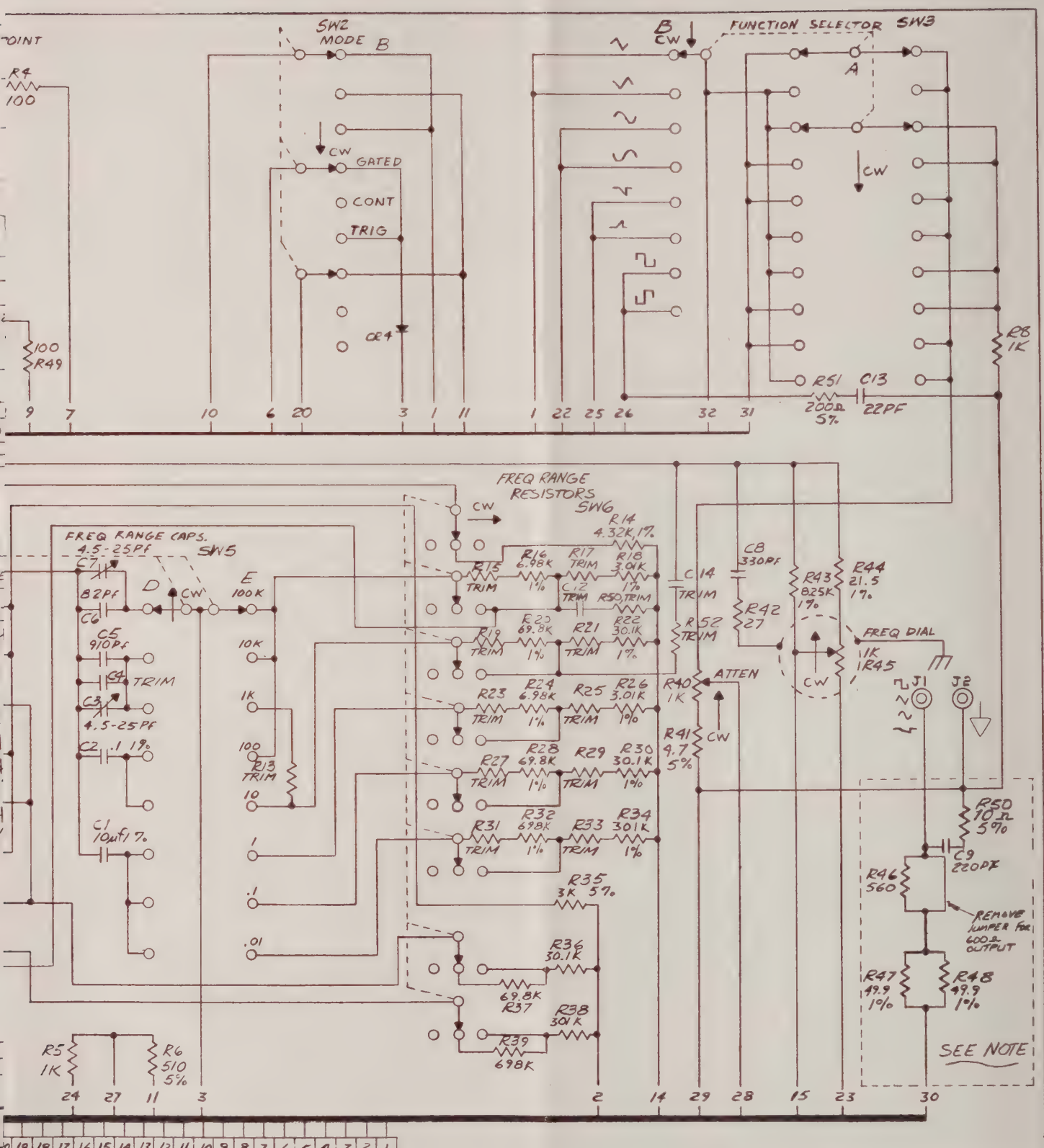
Model 112, 115 & 116. Main Board Assembly (110-012)



NOTE :

FOR "B" MODELS ;

1. REPLACE R46 WITH 430Ω AND REMOVE JUMPER FOR 600Ω OUTPUT.
2. REMOVE C9
3. ADD JUMPER BETWEEN PIN 28 AND 30.
4. PINS NUMBERED FROM RIGHT TO LEFT FROM COMPONENT SIDE



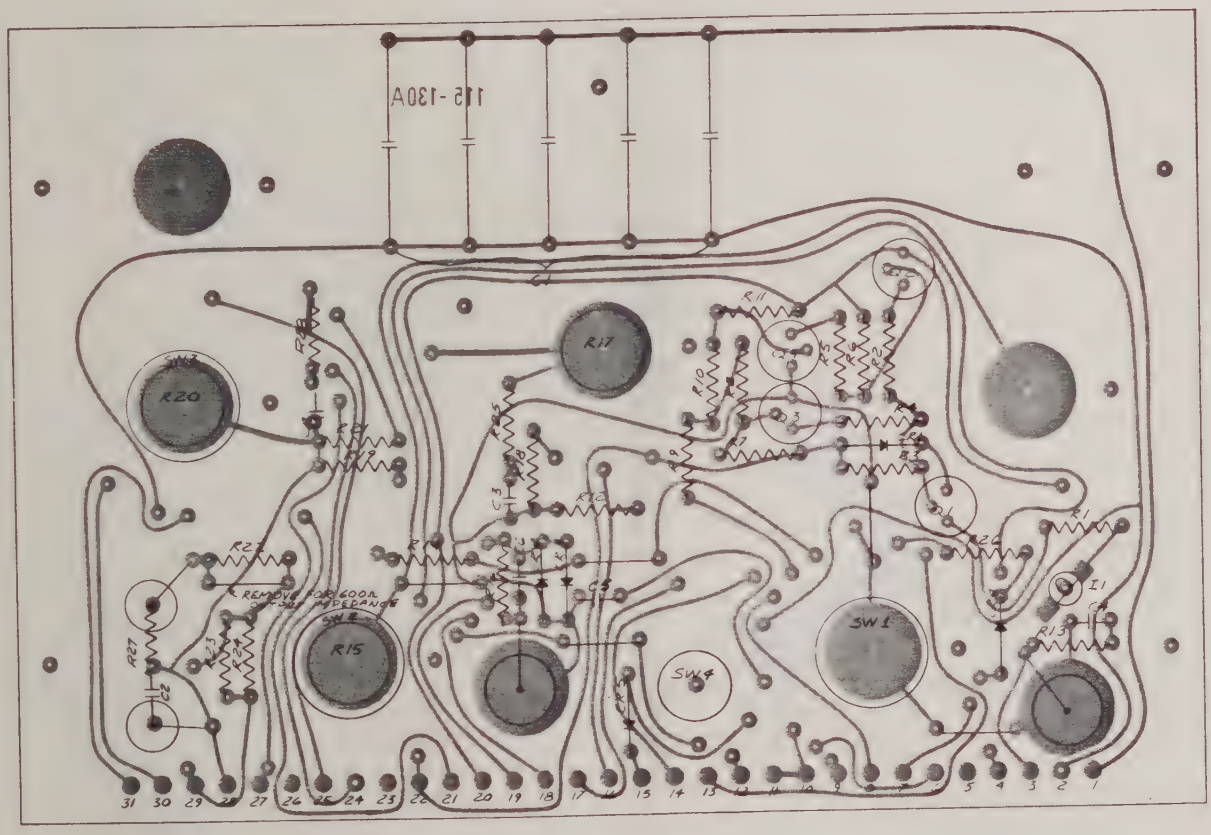
D	ECN #198	ENH	12-12-66	T.O.
C	ECN #173	ENH	9-21-67	T.O.
B	ECN 157	MB	7/20/67	T.O.
A	94 (MRS DWG 112-201C)	JW	12-30-66	T.O.
CHG	ECN NO	BY	DATE	APP'D

WAVETEK SAN DIEGO, CALIF

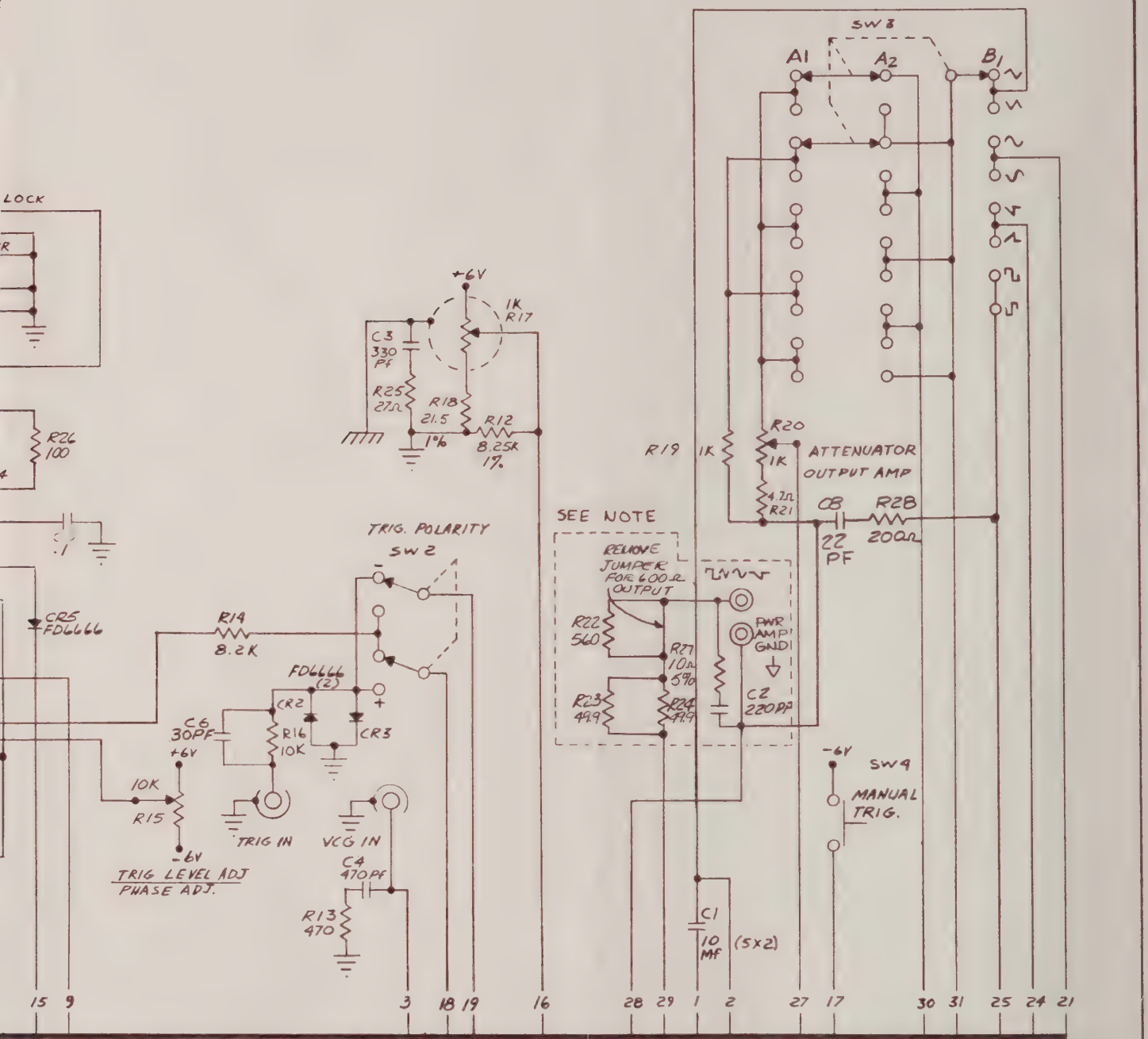
DRN	DATE	APP
PA Monak	5-19-66	

SUB - PANEL

MODEL	NO.
112	C112-2200



Model 115 & 116. Front Panel Assembly (115-030)



D	ECN 155	MBe	7/20/67	
C	ECN # 153	MBe	7/19/67	
B	119	[illegible]	3-22-67	
A	94 (WAS DWG 115-2018)	JW	12-19-66	
CHG	ECN NO.	BY	DATE	APP'D

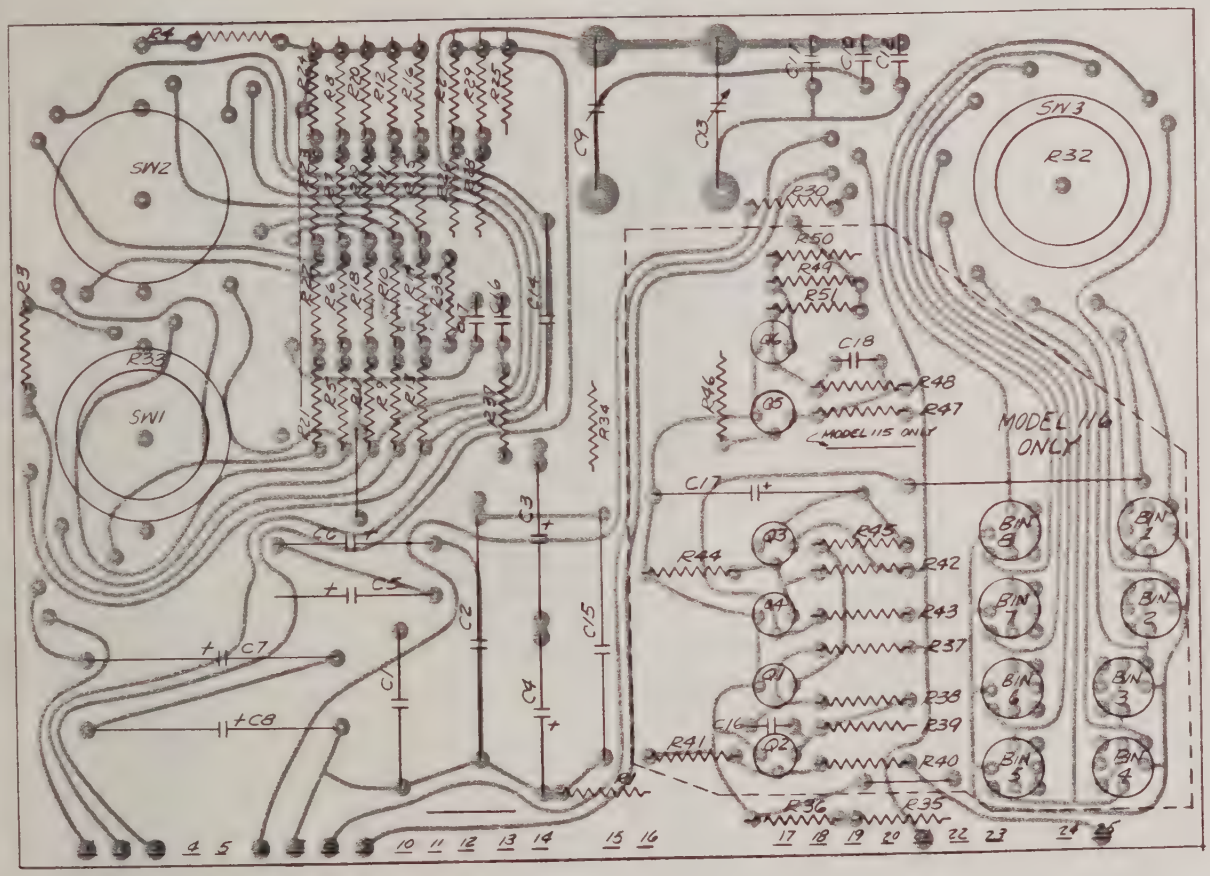
WAVETEK SAN DIEGO, CALIF

DRAWN PA Marsh DATE 5-18-66 APP'D R. Mackie

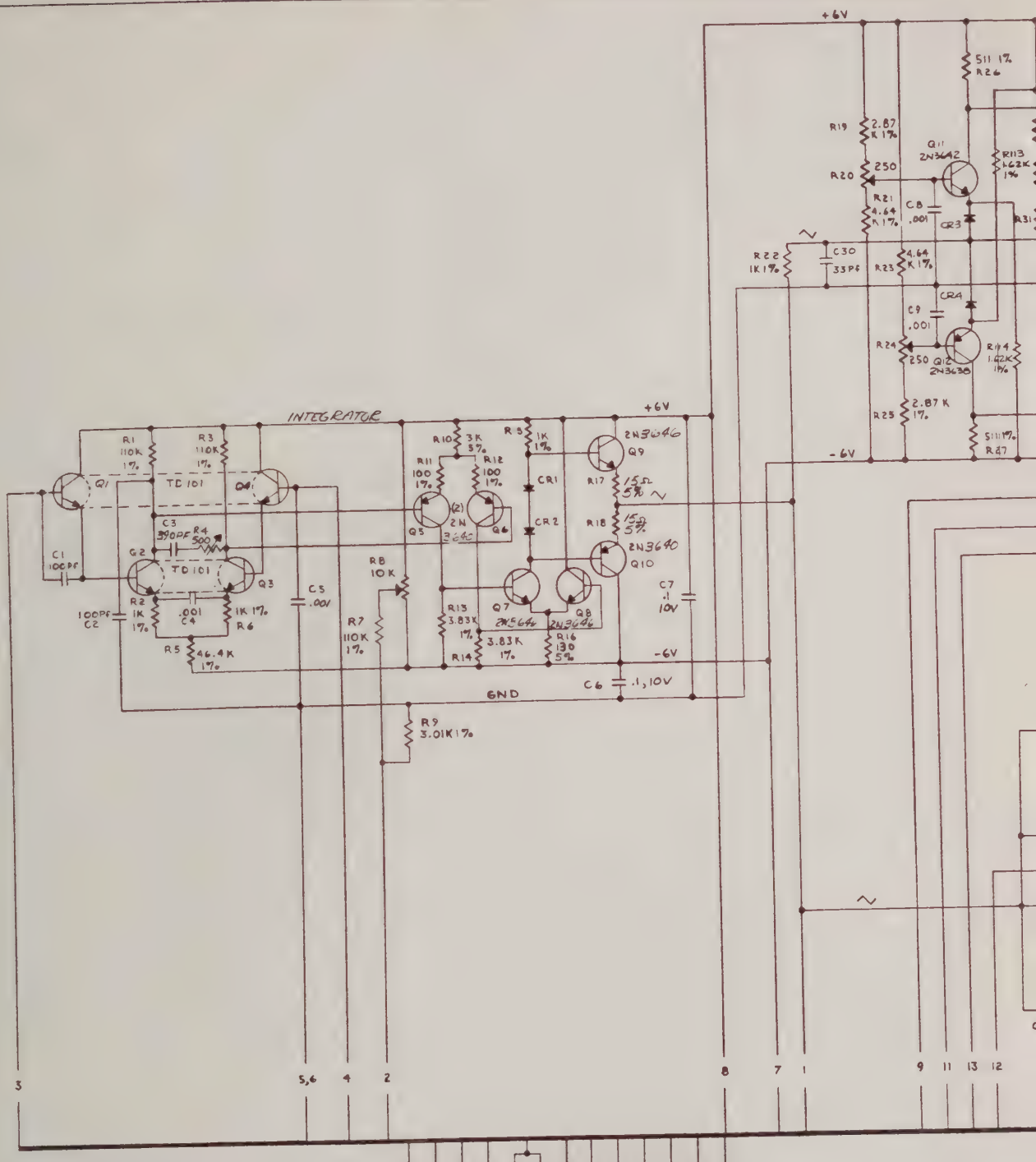
1ST SUB PANEL

MODEL 115-116 NO. 115-230F

F	ECN # 200	MEB	12/21/67	
E	ECN #173	ENH	9-21-67	
CHG	ECN NO.	BY	DATE	APP'D



Model 115 & 116. Second Subpanel Assembly (115-031/116-031)

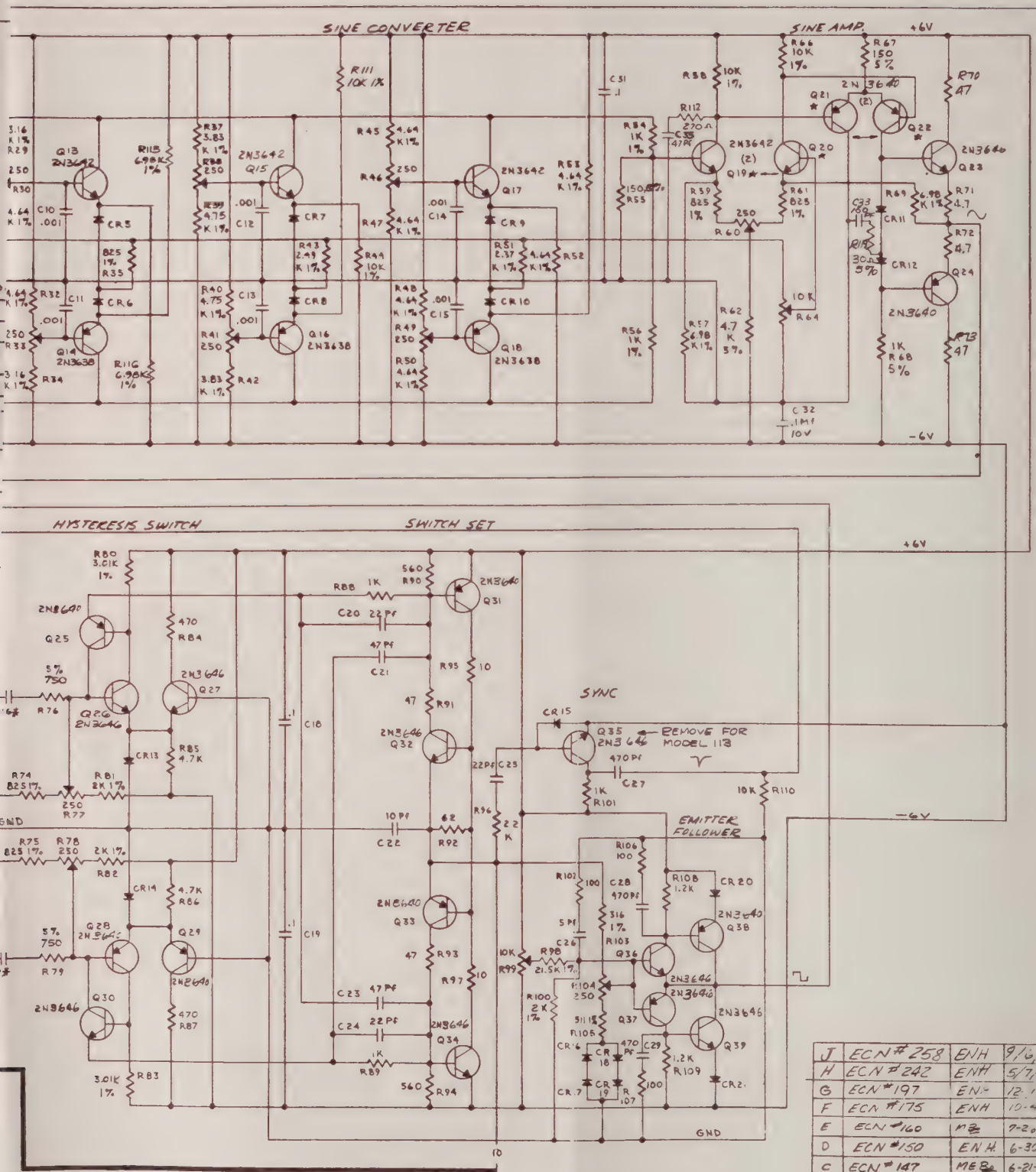


NOTE

UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE IN OHMS, ±10%
2. CAPACITANCE IN MICROFARADS, ±10%
3. DIODES ARE FAIRCHILD FD6666
4. PINS ARE NUMBERED FROM LEFT TO RIGHT AS VIEWED FROM COMPONENT SIDE OF CIRCUIT BOARD
5. * MATCHED PAIR - MATCHED FOR β AND V_{BE}
6. ALL DIFFERENTIAL PAIRS MATCHED FOR 10% β MATCH
7. 6MV; GUARANTEED MINIMUM VALUE
8. Δ INDICATES THERMALLY CONNECTED PAIRS
9. # FOR MODEL 110 USE 220PF; MODEL 113 USE 150 PF, ALL OTHERS USE 100PF.

1 R119
2 C35
3 CR21
4 Q39



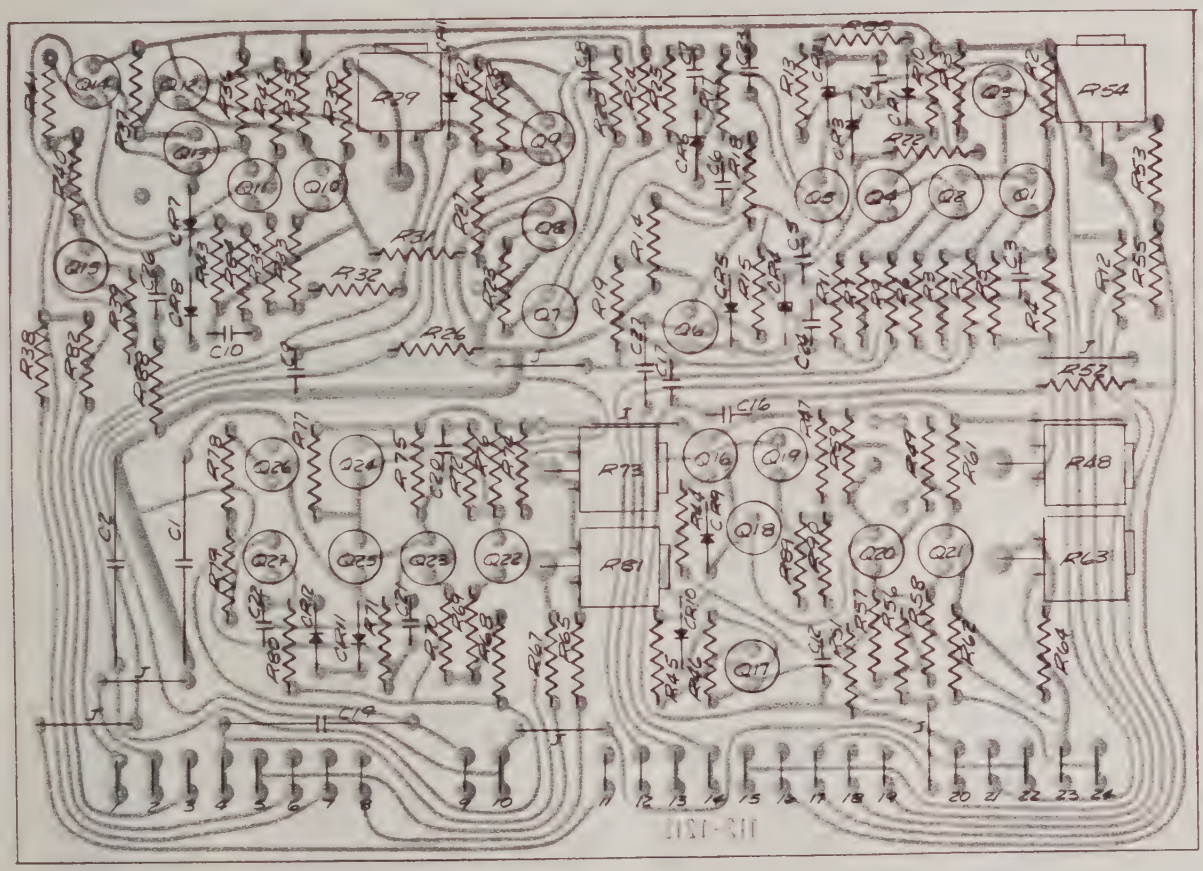
CHG	ECN NO	BY	DATE	APP
J	ECN # 258	ENH	9/6/67	DC
H	ECN # 242	ENH	5/7/67	TC
G	ECN # 197	ENH	12-1-67	TC
F	ECN # 175	ENH	10-4-67	TC
E	ECN # 160	MB	7-20-67	TC
D	ECN # 150	ENH	6-30-67	TC
C	ECN # 147	MEB	6-21-67	TC
B	ECN # 126	JW	3-27-67	AHP
A	ECN # 94 (WAS DWG # 110-202)	JW	12-12-66	TC

WAVETEK SAN DIEGO, CALIF

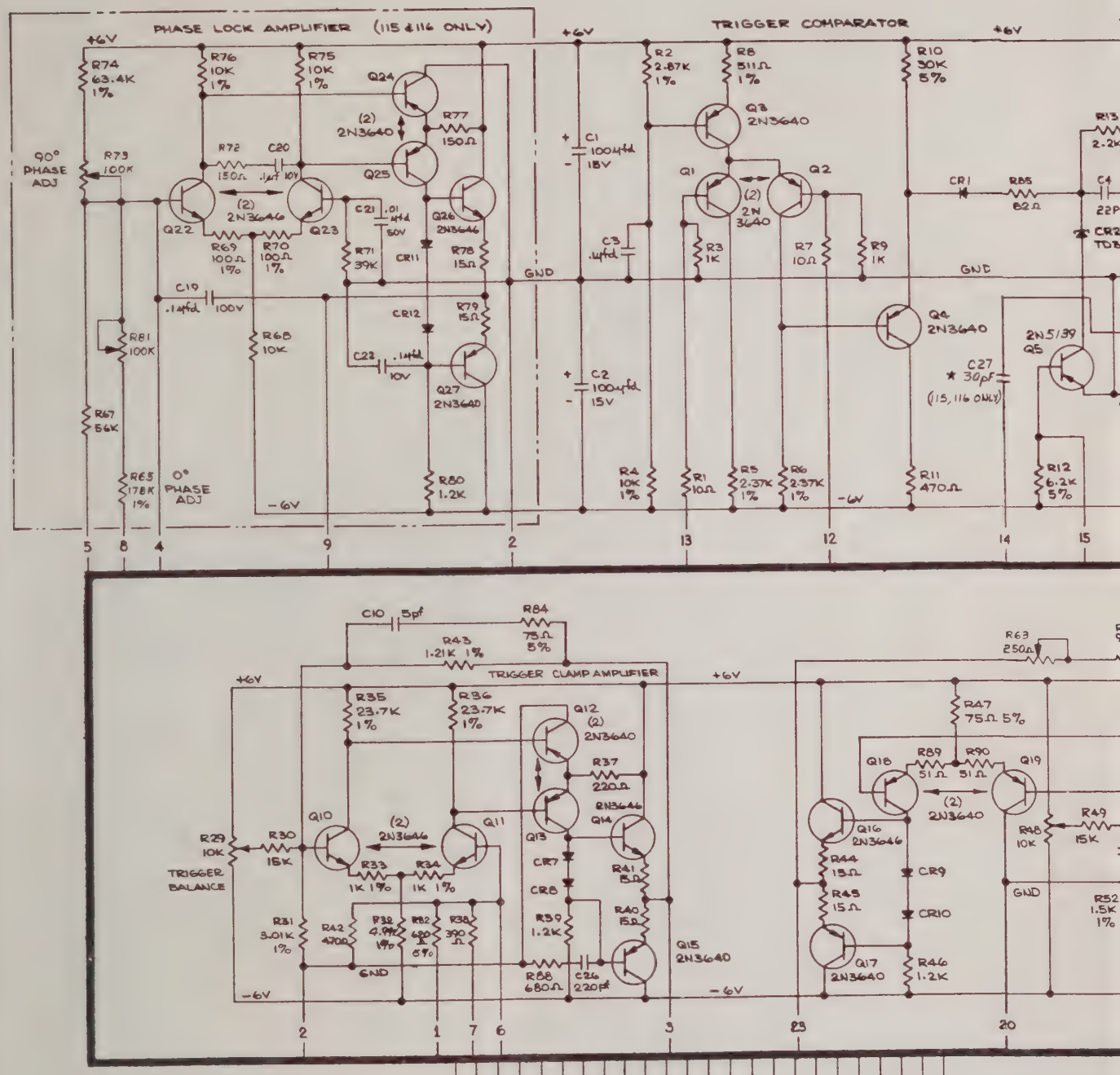
DRN PAMarsh DATE 1-14-66 APP P Mackie

MAINBOARD SCHEMATIC

MODEL 110, 110B, 111, 111B, 112, 112B, 115, 115B, 113 No. D110-212 J



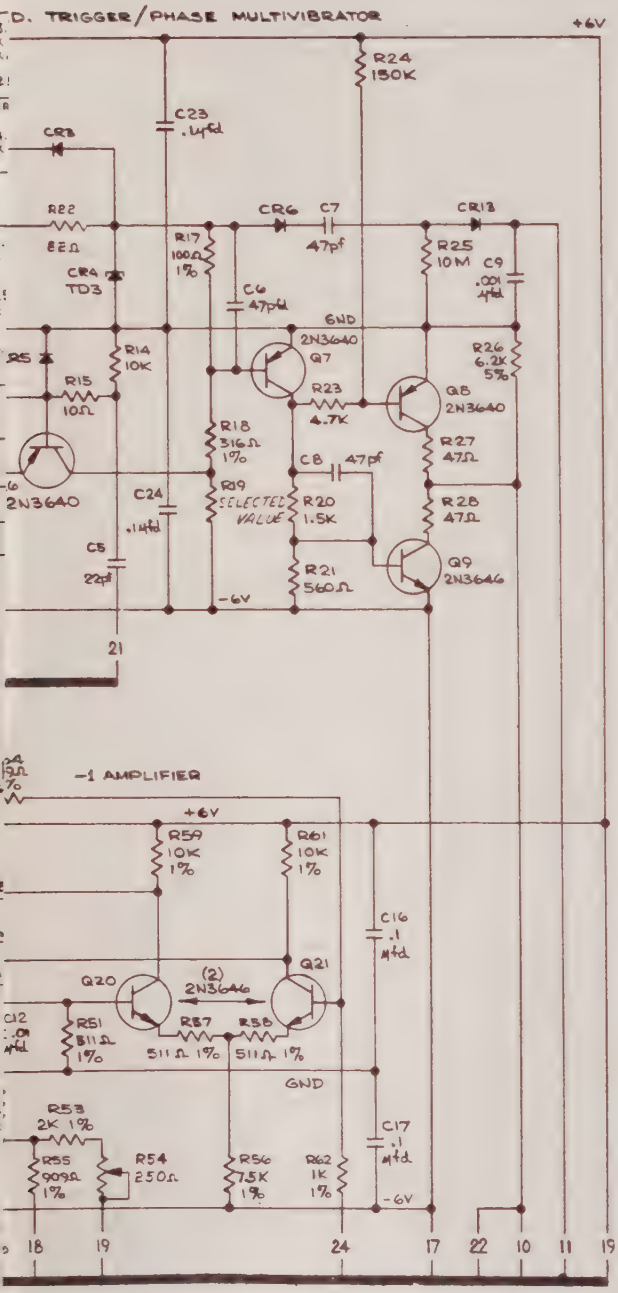
Model 112, 115 & 116. Trigger Board Assembly (112-021)



1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
SS POINT	TRIG GND	TRIG CLAMP AMP OUT	PHASE AMP-IN	PHASE AMP-R IN	TRIG + IN	TRIG + R IN	0° PHASE ADJ	PHASE AMP OUT	TRIG GATE OUT	MANUAL TRIG	+ SLOPE IN	− SLOPE IN	RESET	EXT CYCLE (116 ONLY)	OFFSET ∿ OUT	−6 VDC	∿ IN	+6 VDC	−1 AMP GND	TRIG RESET IN	BINARY RESET OUT	−1 AMP OUT	−1 AMP IN

NOTES:- UNL

1. ALL RESI
2. ALL DIOD
3. ←→ INDIA
4. PINS ARE TO RIGHT COMPONEN BOARD.
5. * SELECT



ESS SPECIFIED
TORS ARE ½W 10%
ES ARE FD6666
ES MATCHED PAIRS
NUMBERED FROM LEFT
AS VIEWED FROM THE
SIDE OF THE CIRCUIT

D VALUE, NOMINAL SHOWN

LATEST COMP DESIGNATOR
R90
C27
CR13
Q27

rev	ecn	by	date	app
L	362	[illegible]	9/25/67	TO
K	CORRECTED ERRORS	FGS	8/25/67	TO
J	# 230	ENH	7/24/67	TO
H	# 205	ENH	7/10/67	TO
G	# 207	ENH	7/24/67	TO
F	# [illegible]	ENH	[illegible]	TO
E	REDRAWN FOR CLARITY	[illegible]	9/11/67	TO
E	# 165	[illegible]	8/2/67	TO
D	# .55	[illegible]	7/17/67	—
C	# 151	ENH	9/24/67	DLP
B	# 137	MEB	5/8/67	—
A	# 94	JW	1/13/67	TO

tolerance unless otherwise specified
.XXX ± .010
XX ± .030

WAVETEK san diego calif

scale N/A | by L. ADAMSON | date 9/11/67 | app [illegible]

material: N/A

finish: N/A

title: TRIGGER BOARD (SCHEMATIC)

model no. 112, 115, 116

dwg no. D112-221

rev L

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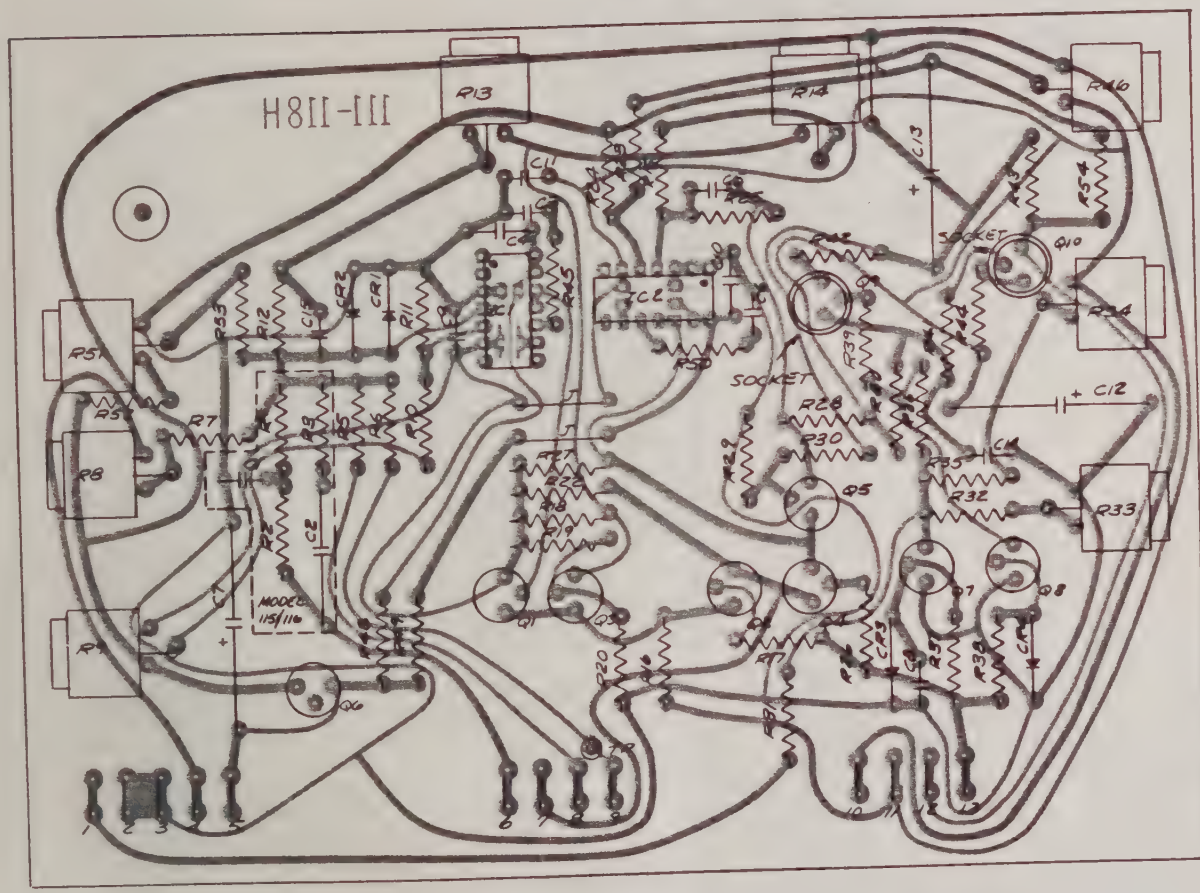
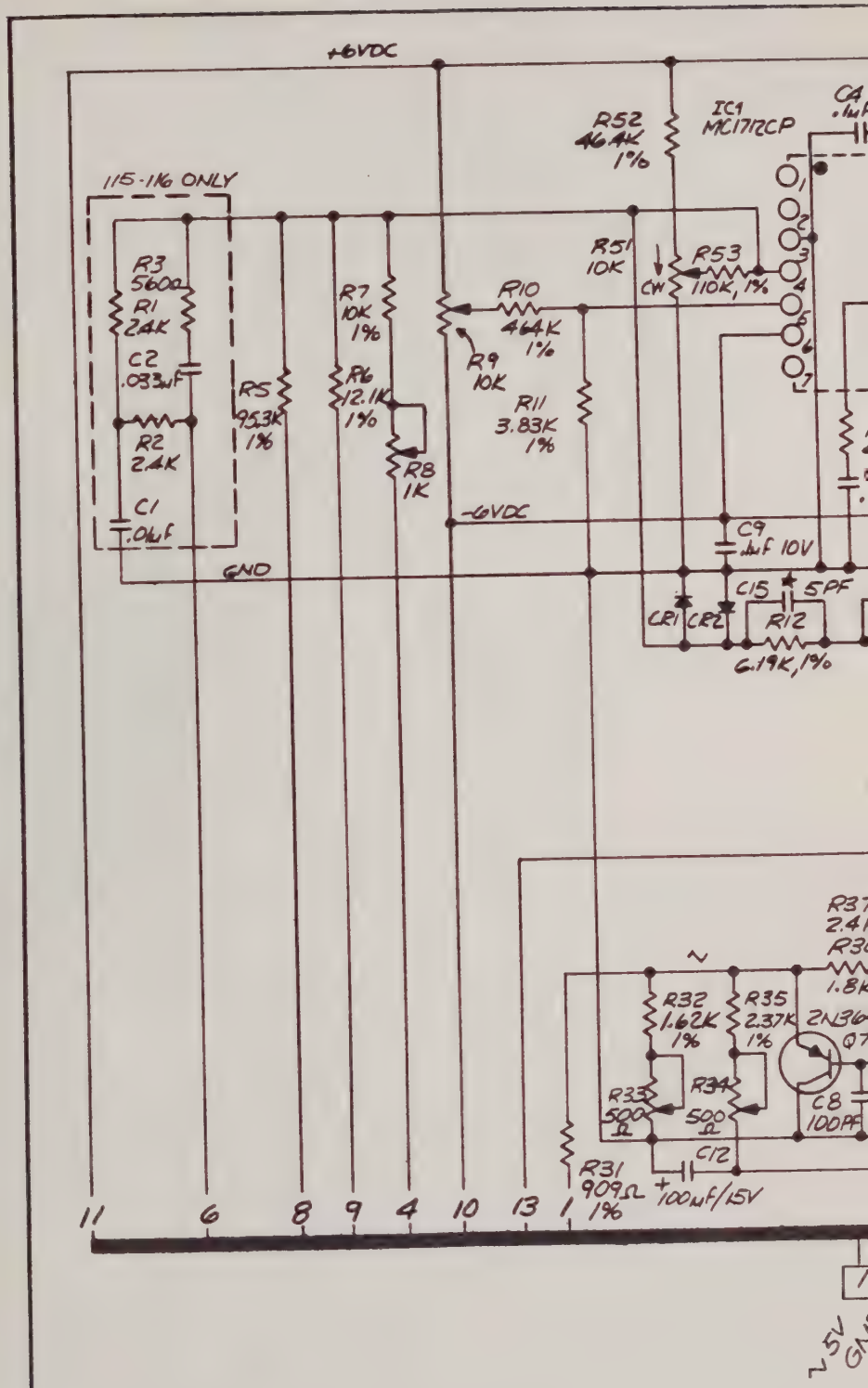


Model 112, 115 & 116. VCG Board Assembly (111-018)



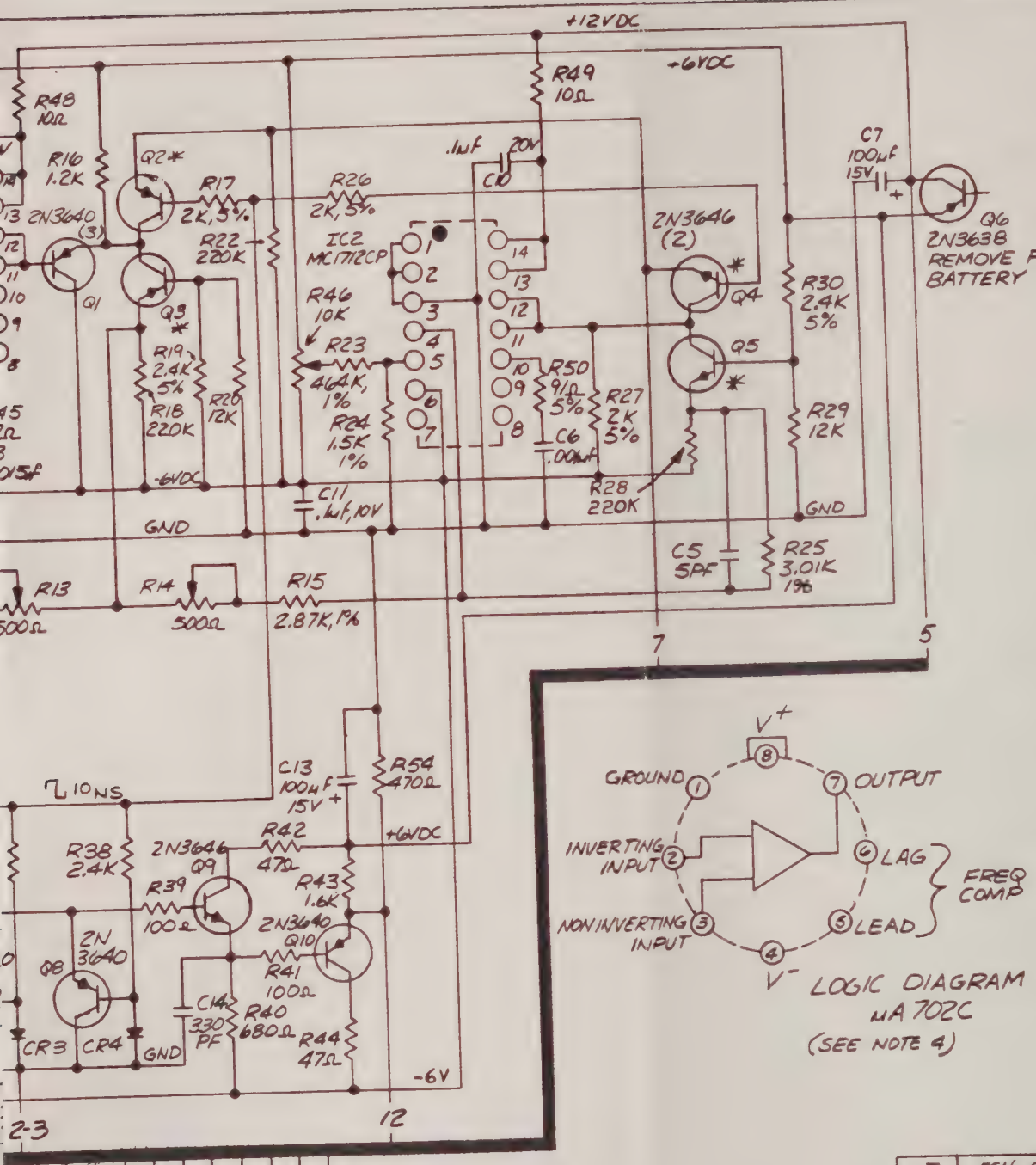
NOTES: UNLESS OTHERWISE SPECIFIED

1 DIODES ARE FOR

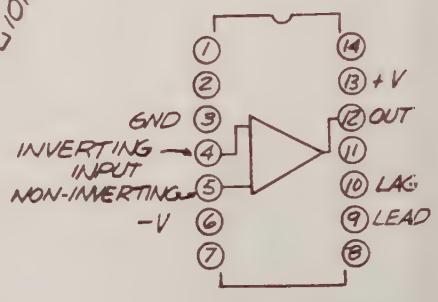
2 * INDICATES MATCHED SPECIAL AS INVERTED SWITCHES

3 ★ INDICATES FOR MODEL 115-176 CHANGE C15 FROM 5PF TO 100PF

4 NA702C MAY BE USED AS AN ALTERNATE FOR MC1712CP



LOGIC DIAGRAM
μA 702C
(SEE NOTE 4)



LOGIC DIAGRAM
MC1712CP

rev	ecn	by	date	app.
T	ECN 284	[illegible]	[illegible]	T.O.
S	CORRECTED ERRORS	FGS	2/25/69	T.O.
R	REDRAWN	BO	2/14/69	T.O.

tolerance unless otherwise specified
.XXX ± .010
.XX ± .030

WAVETEK san diego, calif

scale N/A | by BOCHICHIO | date 2-14-69 | app.

material N/A

title VCG SCHEMATIC

model no 111-116 | dwg no C111-218 | rev T

finish N/A

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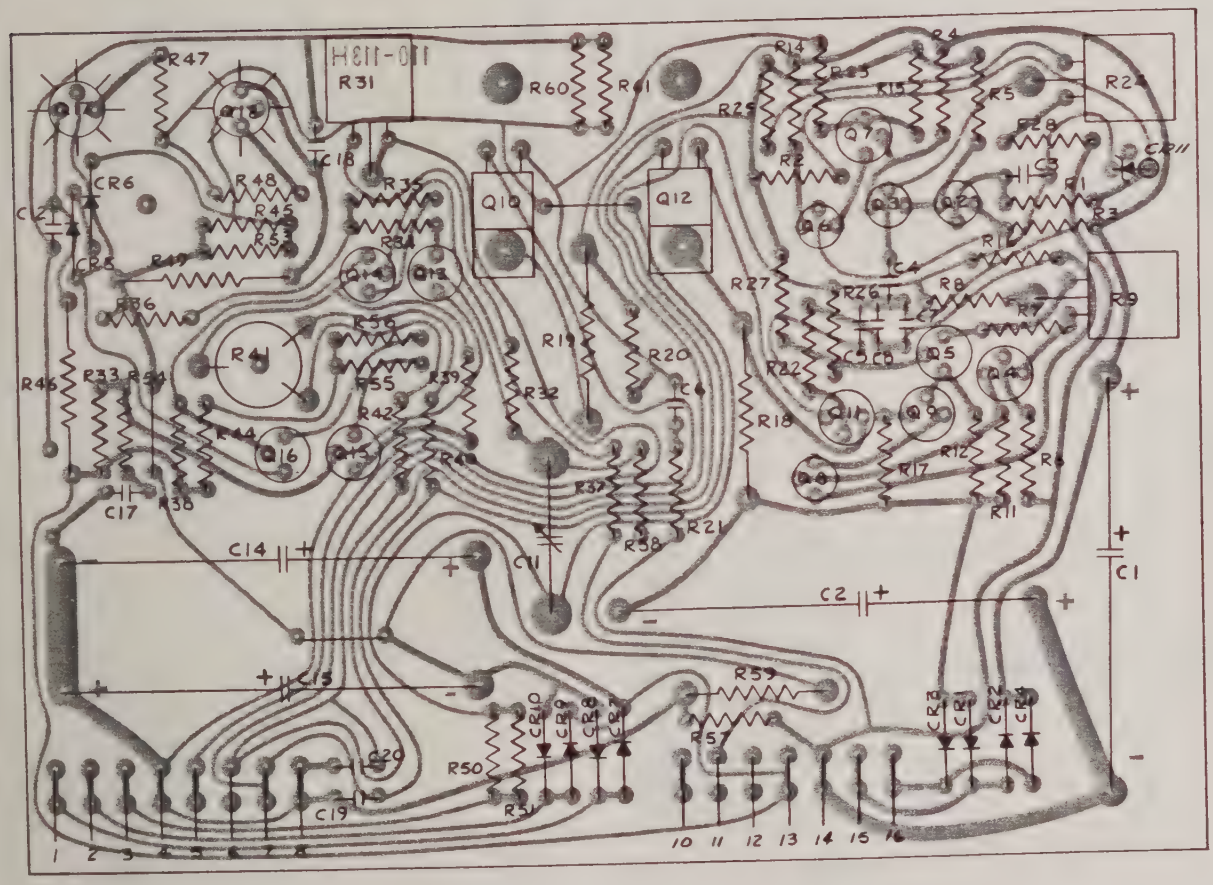
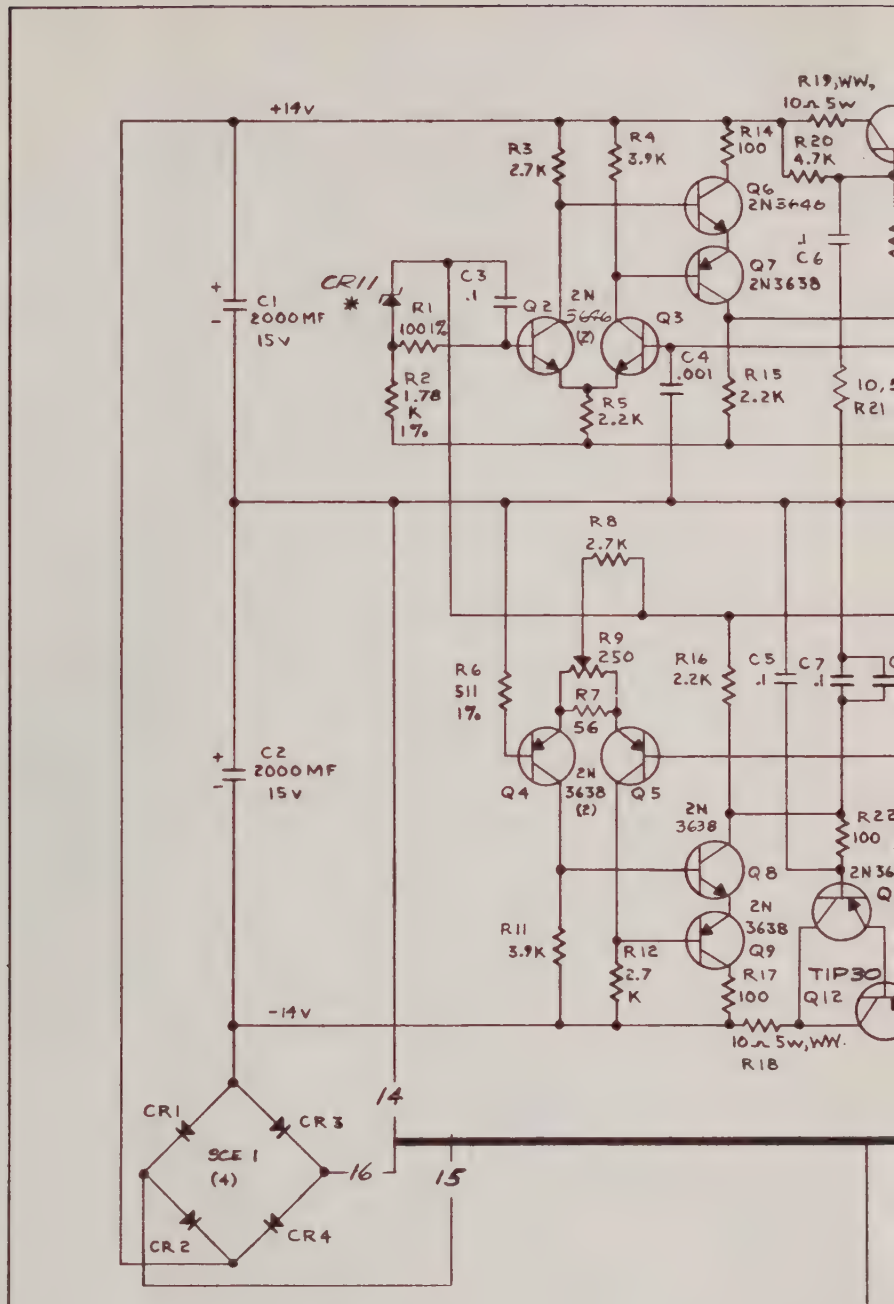


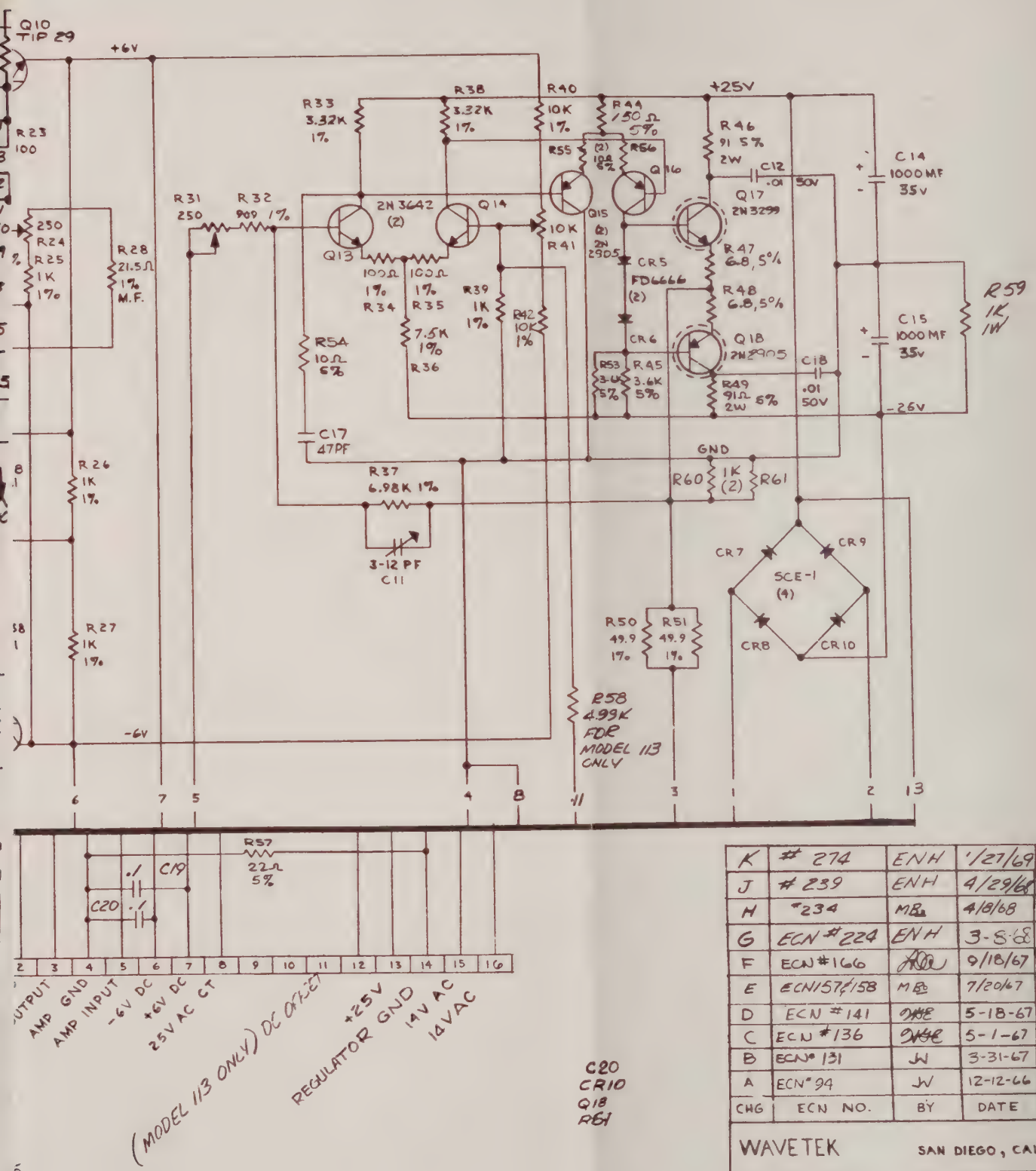
Model 112, 115 & 116. Power Supply and Output Amplifier Assembly (110-013)



NOTE

UNLESS OTHERWISE SPECIFIED :

1. RESISTANCE IN OHMS, ±10%
2. CAPACITANCE IN MICROFARADS, ±10%, 10V
3. * ZENER SELECTED PER WAVETEK SPEC. 130-50
4. PINS ARE NUMBERED FROM LEFT TO RIGHT AS VIEWED FROM COMPONENT SIDE OF CIRCUIT BOARD
5. ALL DIFFERENTIAL PAIRS MATCHED FOR 10% β MATCH



CHG	ECN NO.	BY	DATE	APP
K	# 274	ENH	1/27/69	T.O
J	# 239	ENH	4/29/68	T.O.
H	#234	MB	4/18/68	T.O.
G	ECN #224	ENH	3-8-68	T.O.
F	ECN #166	[illegible]	9/18/67	T.O
E	ECN157,158	MB	7/20/67	T.O.
D	ECN #141	[illegible]	5-18-67	[illegible]
C	ECN #136	[illegible]	5-1-67	[illegible]
B	ECN° 131	JW	3-31-67	[illegible]
A	ECN° 94	JW	12-12-66	[illegible]

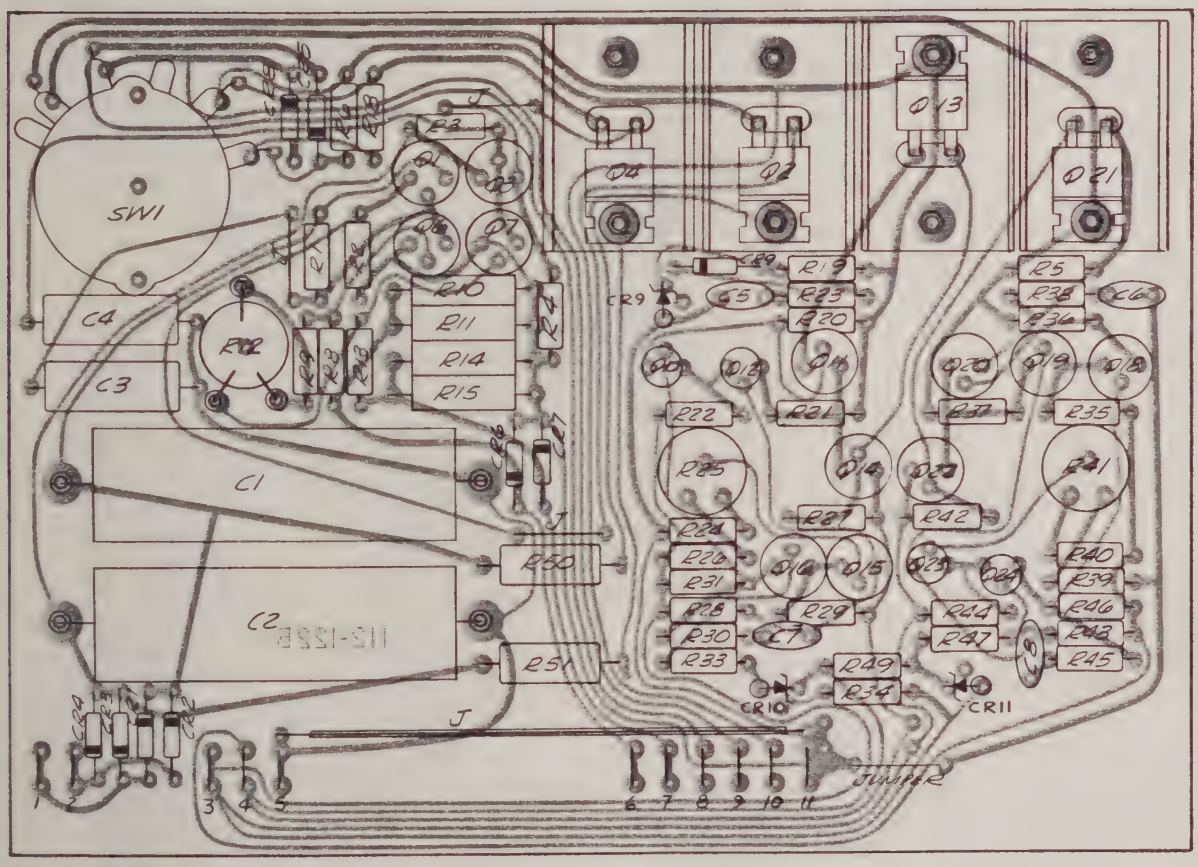
WAVETEK SAN DIEGO, CALIF

DRN DATE: PA Marsh 1-21-66 APP: P. Martin

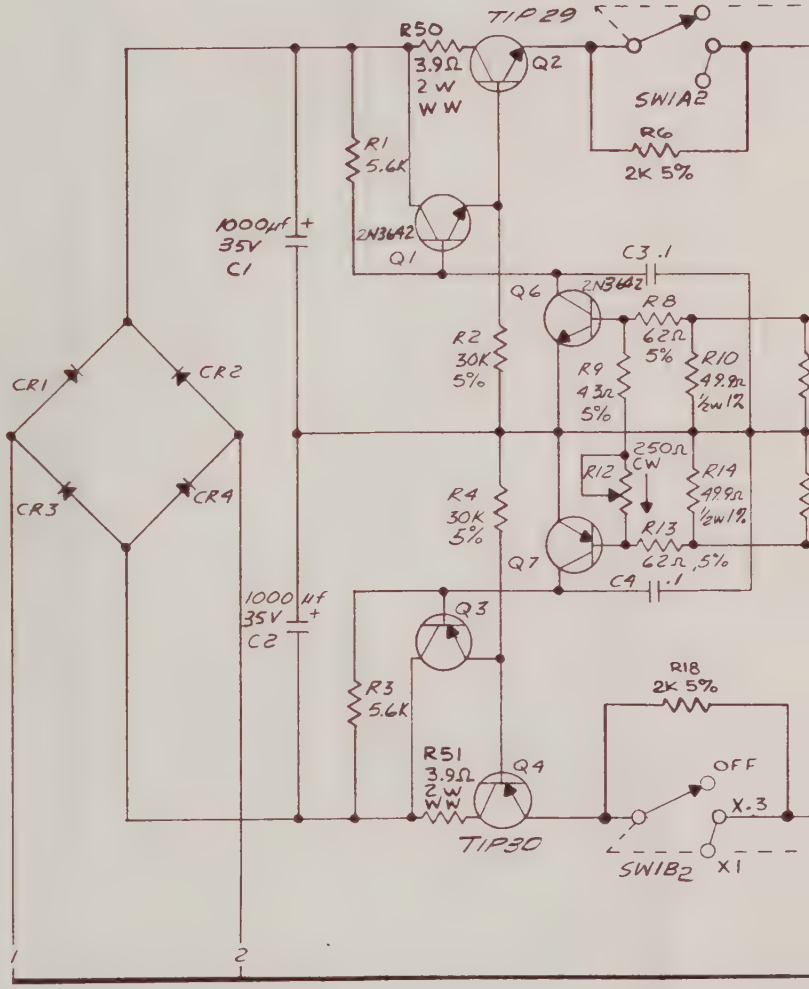
POWER SUPPLY AND OUTPUT AMP

MODEL 110 THRU 116 NO. C110-213 N

CHG	ECN NO.	BY	DATE	APP
N	ECN 339	TRQ	3/18/71	T.O
M	ECN 279	[illegible]	7/30/69	T.O
L	CORRECTED ERRORS	FGS	2/25/69	T.O

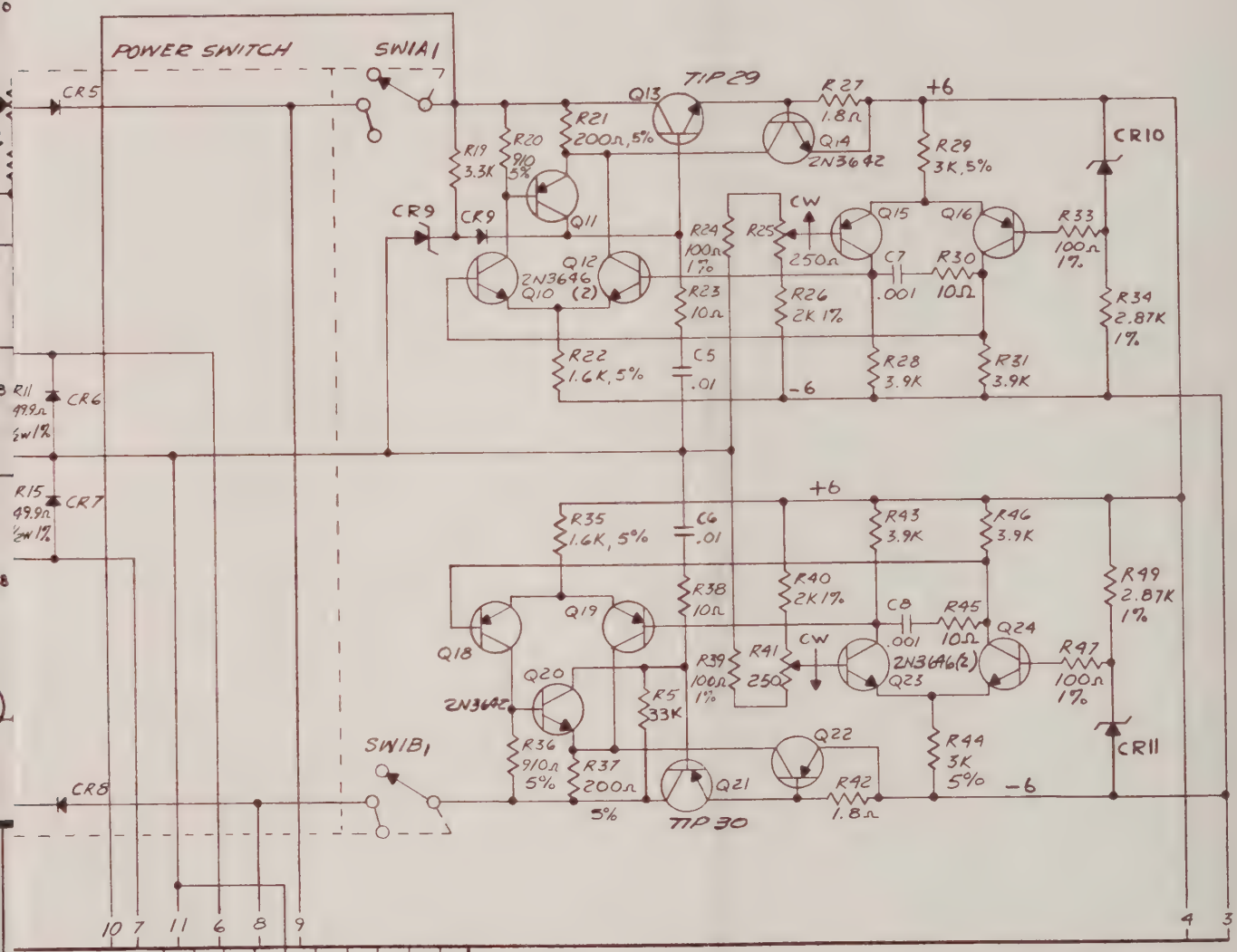


Model 112B, 115B & 116B. Battery Regulator Assembly (112-022)



NOTE: UNLESS OTHERWISE SPECIFIED

1. ALL TRANSISTORS ARE 2N3638
2. ALL RESISTANCE IN OHMS, ½W, 10%
3. CAPACITANCE IN MICROFARADS
4. DIODES ARE SCE-1's.
5. PINS NUMBERED LEFT TO RIGHT AS VIEWED FROM COMPONENT SIDE OF BOARD.
6. ALL DIFFERENTIAL PAIRS ARE MATCHED FOR β
7. ZENER DIODES SELECTED PER WAVETEK SPEC 130-506(CR
8. TRANSISTORS 2N3740 AND 40250 ARE INTERCHANGABLE ALTERNATES WITH TIP 29 AND TIP30 RESPECTIVELY



LATEST COMP DESIGNATOR
R51
C 8
CR 11
Q25

9,10,11)

CHANGE	ECN NO.	BY	DATE	APP'D
F	ECN 291	[illegible]	1-6-70	T.O.
E	CHG WAFER *	FGS	3-6-69	T.O.
D	ECN #167	ENH	9-5-67	T.O.
C	153	MES	7/18/67	T.O.
B	ECN * 152	[illegible]	7/11/67	T.O.
A	94 (MAS DWG 1128-105)	JW	1-5-67	T.O.

WAVETEK SAN DIEGO, CALIF

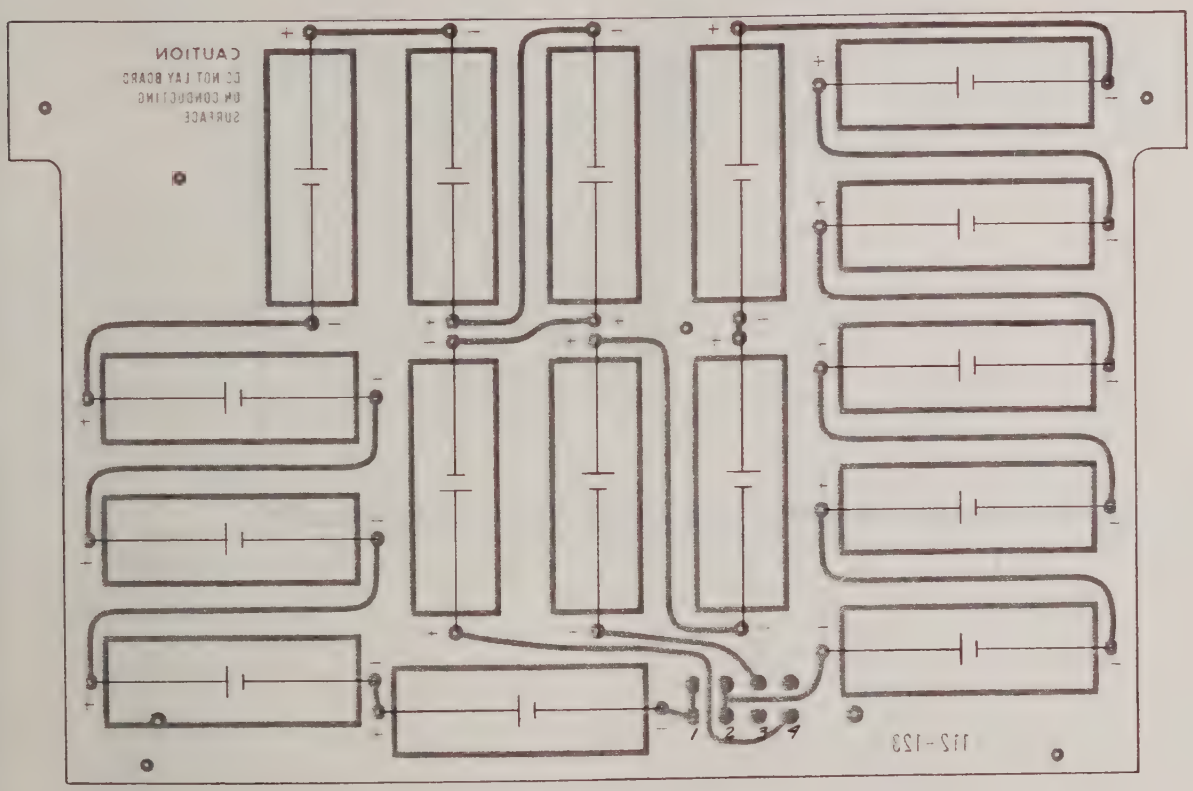
DRN PA Marsh DATE 7-21-66 APP'D P. Mackie

BATTERY REGULATOR BD

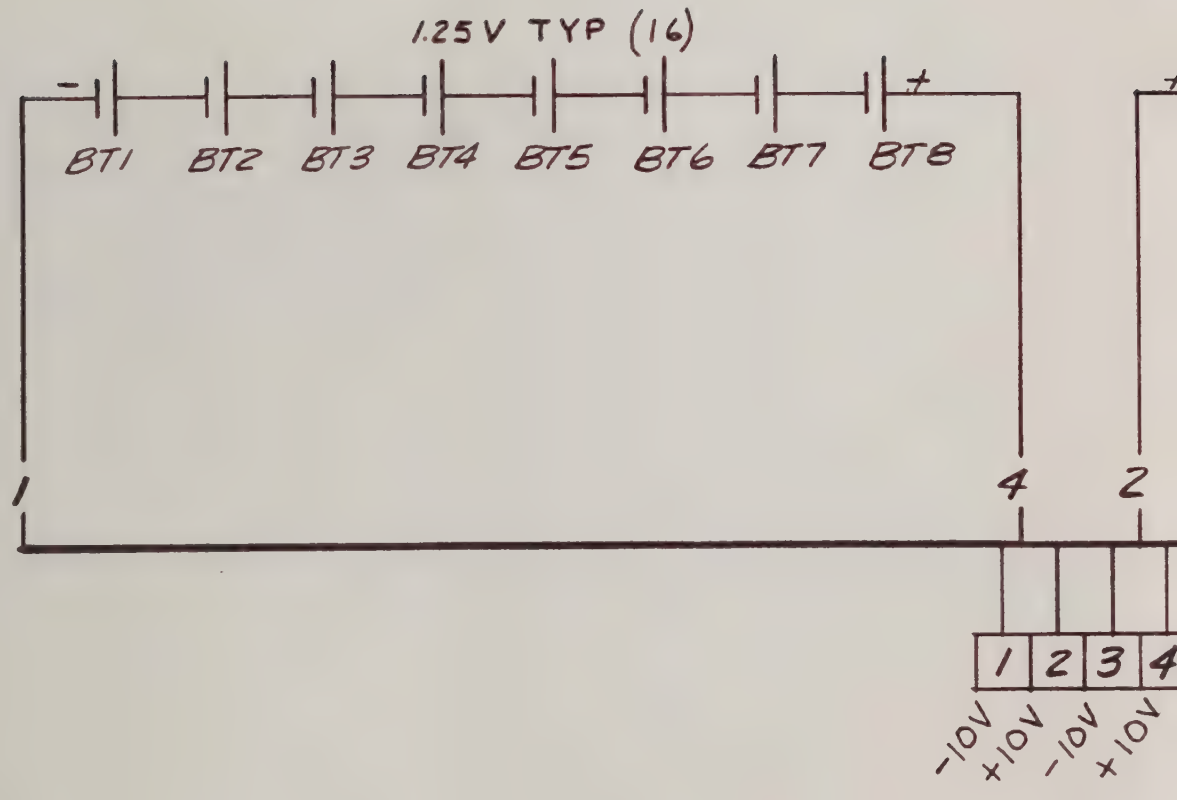
CHG	ECN NO.	BY	DATE	APP'D
G	ECN 281	NG	12-16-70	T.O.

MODELS 110-116

NO C112-2226



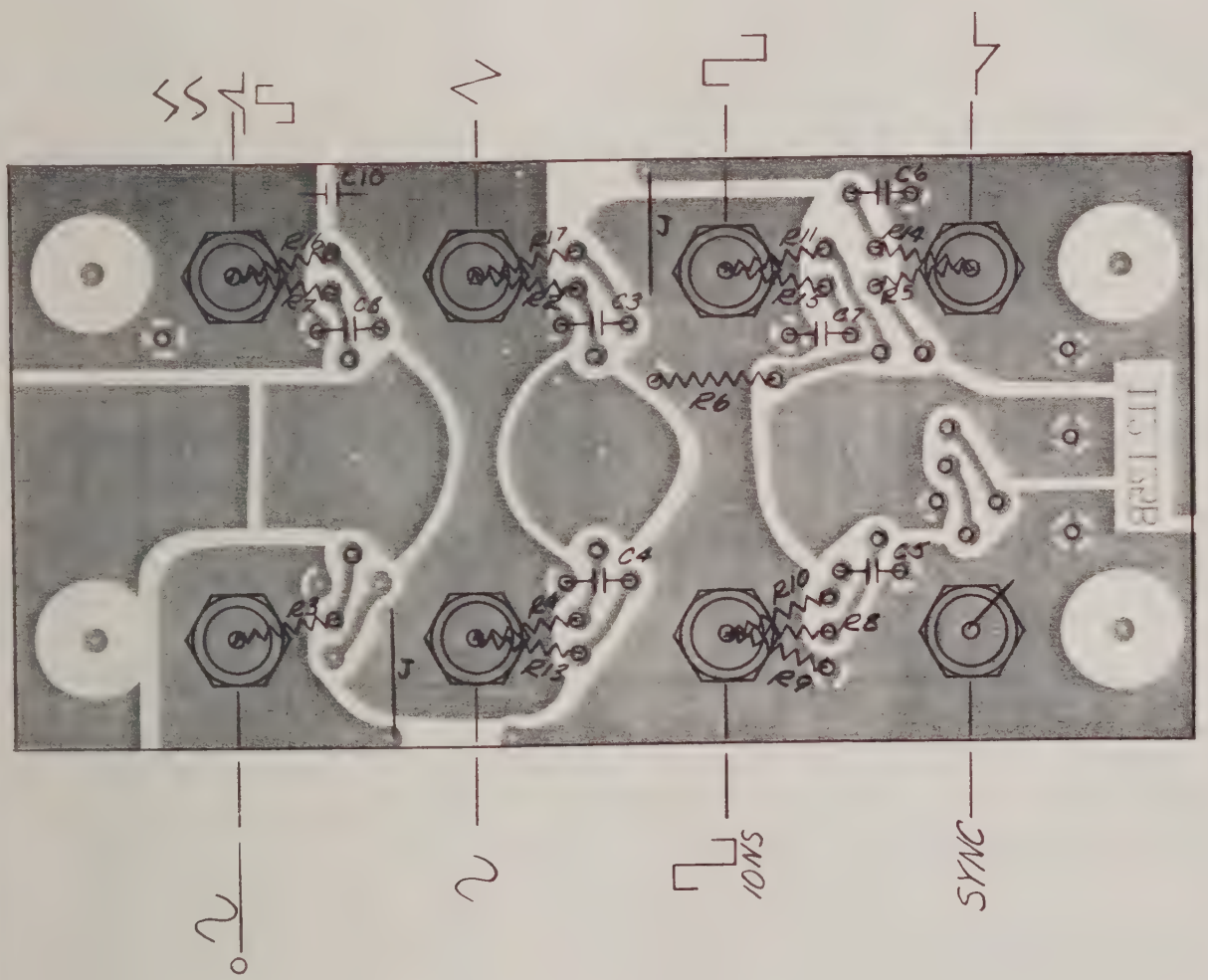
Model 112B, 115B & 116B. Battery Pack Assembly (112-023)


1.25V TYP (16)
-
+
BT1
BT2
BT3
BT4
BT5
BT6
BT7
BT8
1
4
2
1
2
3
4
-10V
+10V
-10V
+10V

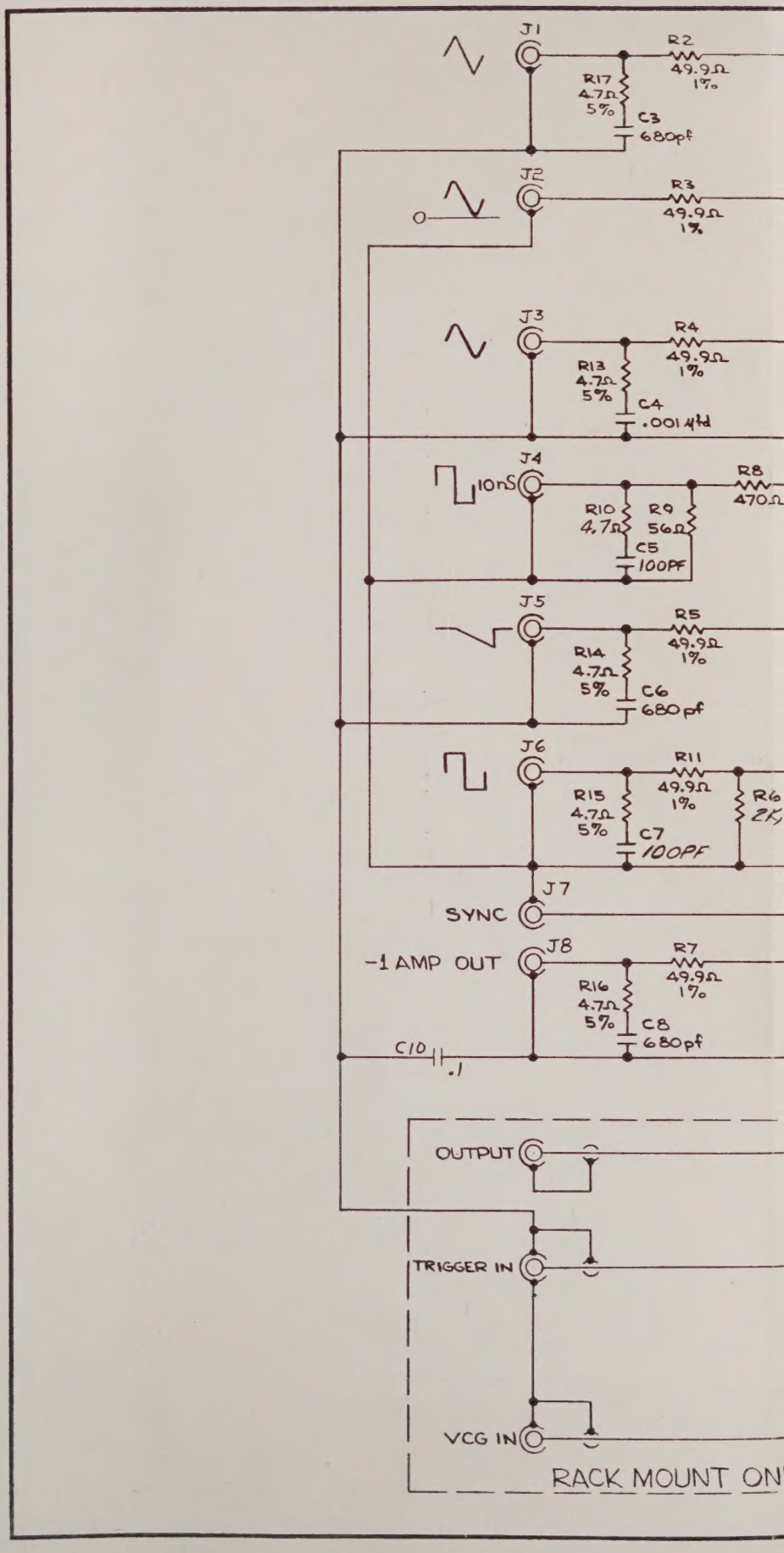
WAVETEK	SAN DIEGO, CALIF.
DWN: WHITELOCK DATE: 1-16-67	APP'D: P. Mackie

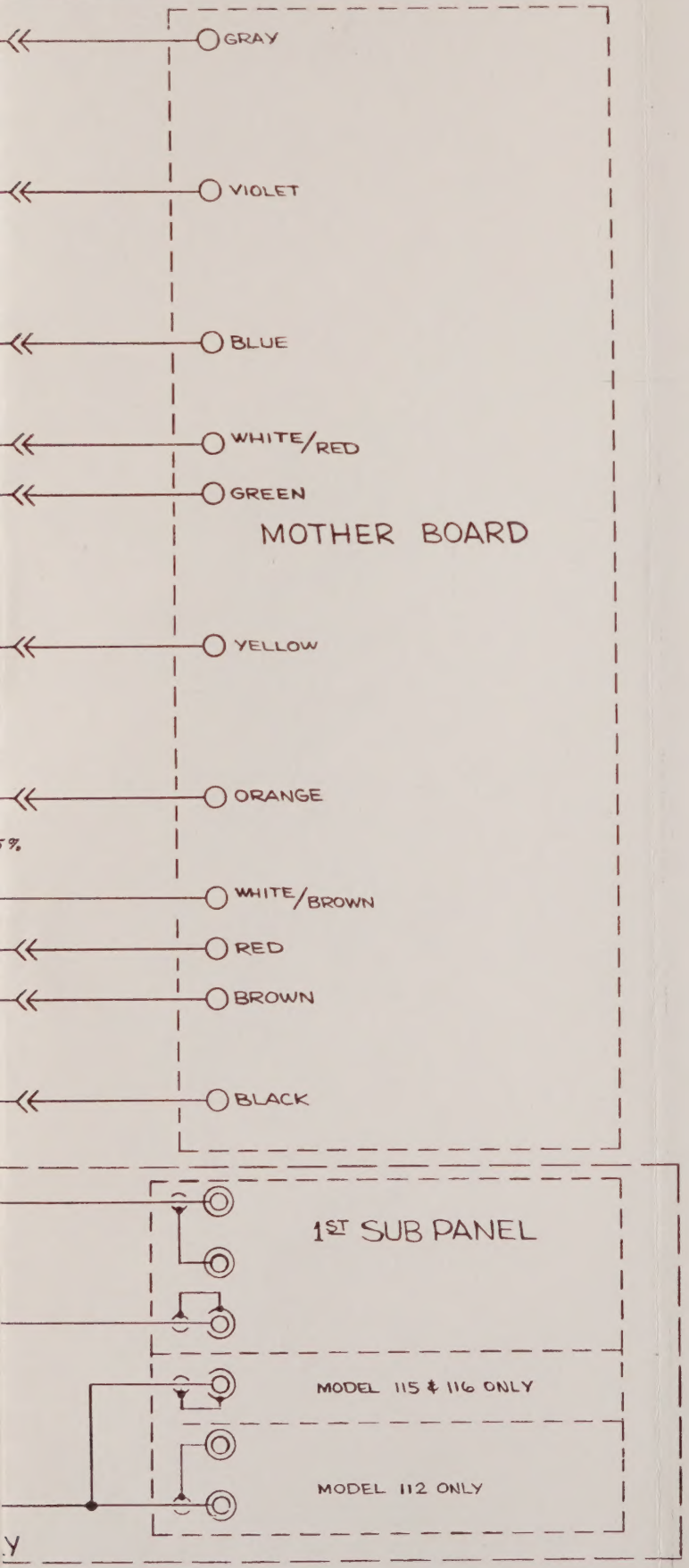
SCHEMATIC - BATTERY PACK

MODEL: 110-116	NO. 112-223



Model 112, 115 & 116. Connector Mounting Board Assembly (112-025)


J1
R2
49.9Ω
1%
R17
4.7Ω
5%
C3
680pf
J2
R3
49.9Ω
1%
J3
R4
49.9Ω
1%
R13
4.7Ω
5%
C4
.001μf
J4
10nS
R8
470Ω
R10
4.7Ω
R9
56Ω
C5
100PF
J5
R5
49.9Ω
1%
R14
4.7Ω
5%
C6
680pf
J6
R11
49.9Ω
1%
R15
4.7Ω
5%
C7
100PF
R6
2K
J7
SYNC
J8
-1 AMP OUT
R7
49.9Ω
1%
R16
4.7Ω
5%
C8
680pf
C10
.1
OUTPUT
TRIGGER IN
VCG IN
RACK MOUNT ON



rev	ecn	by	date	app.
D	ECN #248	ENH	4/19/68	T.O
C	ECN #200	ENH	4/14/68	T.O
B	ECN #198	ENH	12/7/67	T.O.
A	ECN #166	[illegible]	9/6/67	T.O.

tolerance unless otherwise specified
.XXX ± .010
.XX ± .030

WAVETEK san diego, calif

scale N/A | by L. ADAMSON | date 9/6/67 | app. [illegible]

material: N/A

finish: N/A

title: CONNECTOR MOUNTING BOARD (SCHEMATIC)

model no.	dwg no.	rev
112,115,116	C112-225	D

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